1 Cover Sheet
2 System Block Diagram
3 Intel LGA775 CPU - Signals
4 Intel LGA775 CPU - Power
5 Intel LGA775 CPU - GND
6 nVidia C73 - CPU / PCI-E
7 nVidia C73 - HT Link / Power
8 nVidia C73 - Memory A0
9 nVidia C73 - Memory A1
10 nVidia C73 - Gnd
11 DDR II DIMM 1 & 2
12 DDR II DIMM 3 & 4
13 PCIE RESET
14 nVidia MCP55 - HT / PCI / LPC
15 nVidia MCP55 - PCI-E
16 nVidia MCP55 - SATA / IDE / RGMII
17 nVidia MCP55 - Audio / USB / GPIO
18 nVidia MCP55 - PWR & GND
19 NB PCI-E x16 Pri / Sec Slot
20 SB PCI-E x16 Pri / Sec Slot
21 SB PCI-E x1 / PCI Slot
22 Gigabit PHY - RTL8211B
23 1394 Controller - JMB381
24 Azalia Codec - ALC888
25 JMicron JMB363
26 Super I/O - F71882FG
27 Fan Controller
28 uPI ACPI Solution
29 uPI Power Regulator
30 VRD11- ISL6322 8 Phase
31 Front / Rear USB Connectors
32 ATX / Front Panel / LED
33 Manual Parts
34 Power On/Off Sequence
35 System Reset Map
36 Syatem Power Map
37 GPIO & Jumper Setting
38 Project History

MS-7523 Version : 0A *Diamond Edition*

CPU :

Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 Sequence

System Chipset :

nVidia C73
nVidia MCP55P

On Board Chipset :

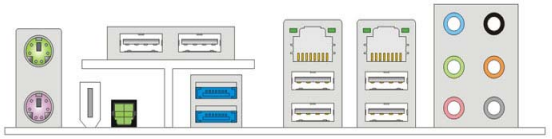
Azalia Codec - RealTek ALC888
GB PHY 1 -- RealTek RTL8211BL
GB PHY 2 -- RealTek RTL8211BL
VRM 11 - Intersil ISL6322
ACPI Controller -- uPI Solution
IEEE 1394a Controller -- JMicron JMB381
eSATA Controller -- JMicron JMB363
Super I/O -- FinTek F71882FG
SPI Flash 8Mb

Main Memory :

2 Channel DDR III* 4 (Max 8GB)

Expansion Slot :

PCI Express x16 Slot * 3
PCI Express x8 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1



ERP No.	Config Item	PlatForm or Option	Option Select
7510-01S	Cfg-STD	C55 + BR04 + MCP55P + ALC885 + RTL8211BP + JMB381 + JMB363 + F71882FG	STD

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	Cover Sheet	
Size	Document Number MS-7523	Rev 0A
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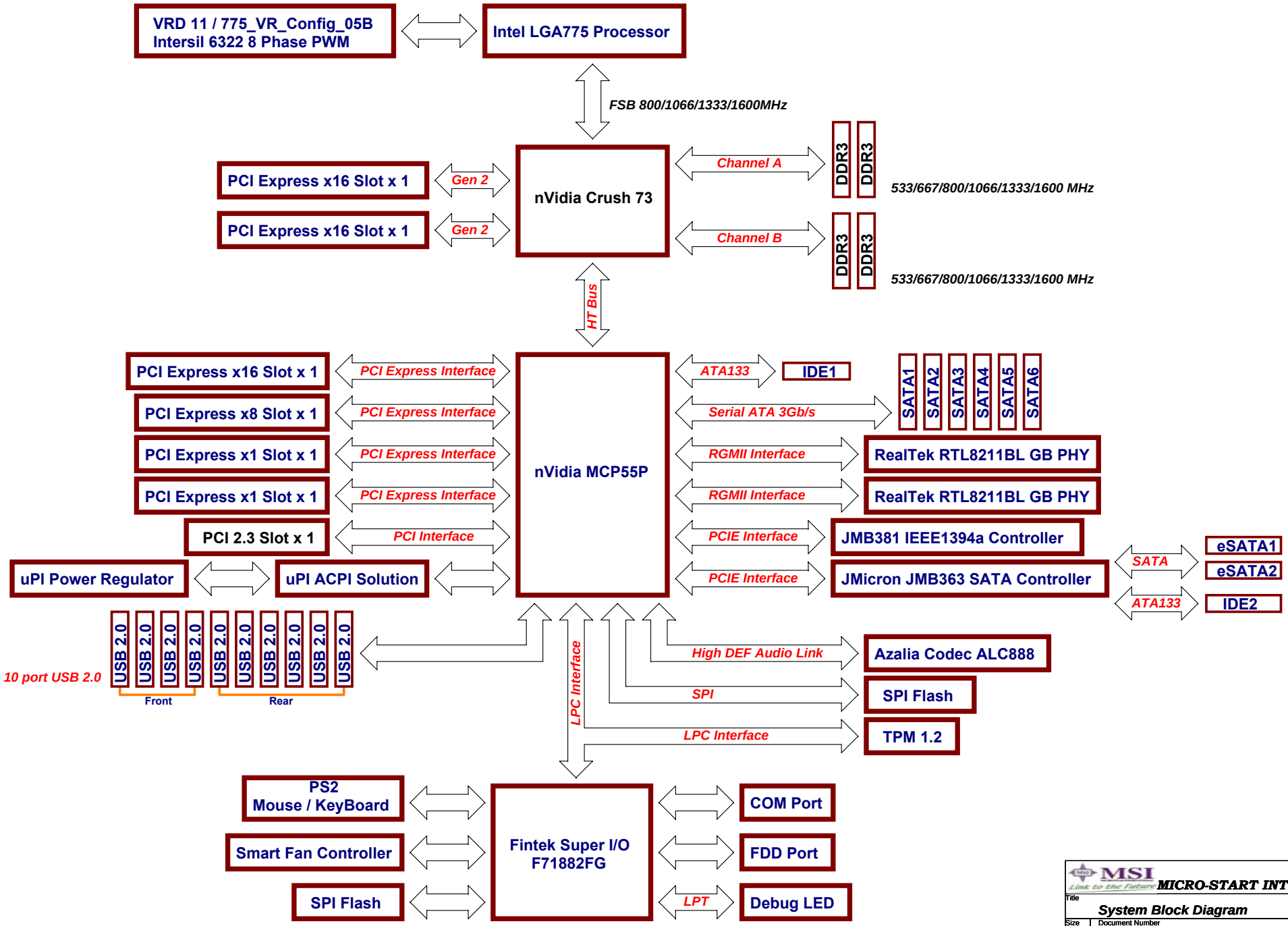
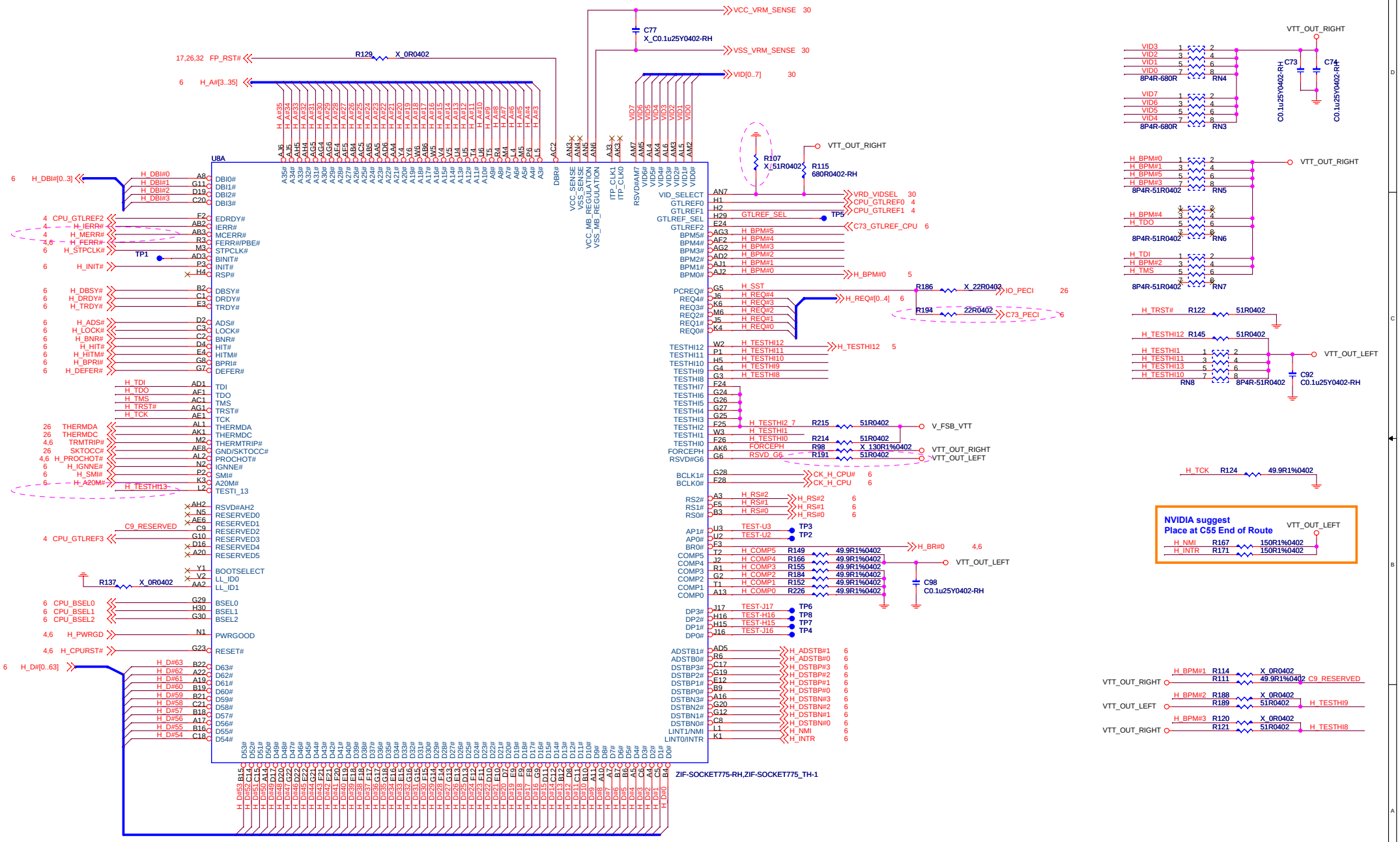
System Block Diagram



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	System Block Diagram	
Size	Document Number MS-7523	Rev 0A
Date: Friday, November 30, 2007	Sheet 2 of 38	

CPU LGA775 - Signals



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title		
CPU LGA775 - Signals		
Size	Document Number	Rev
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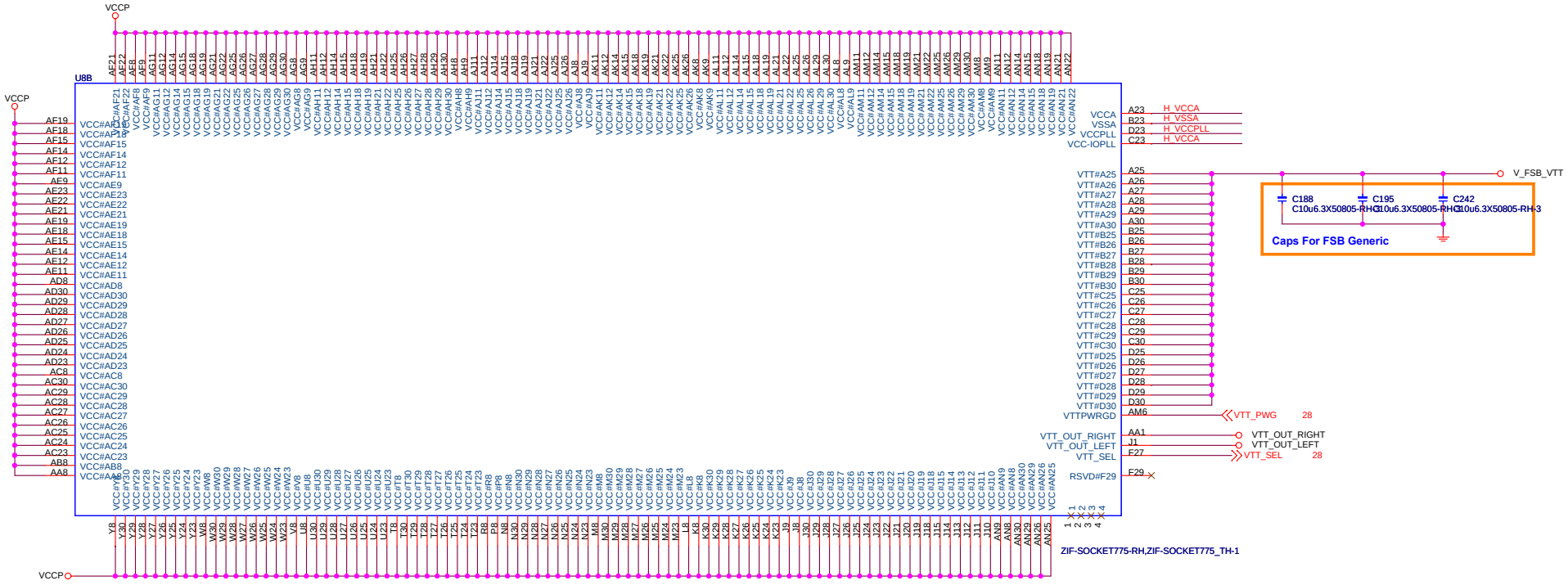
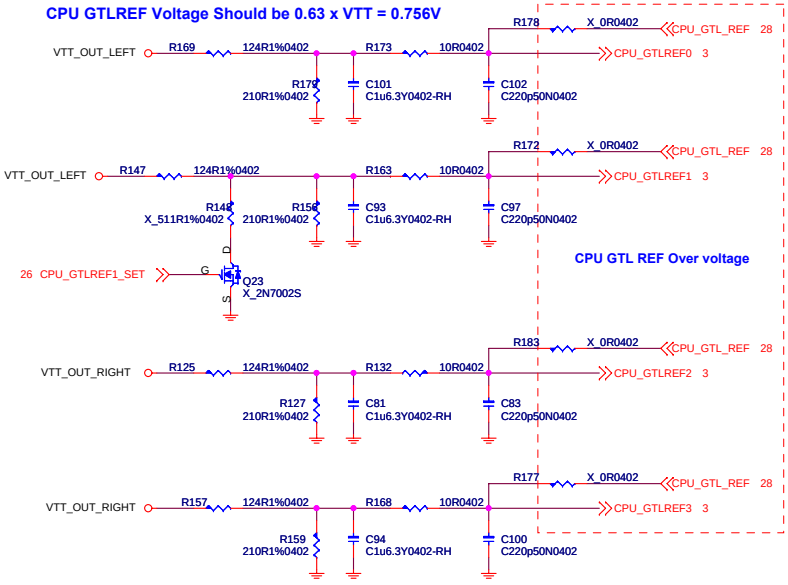
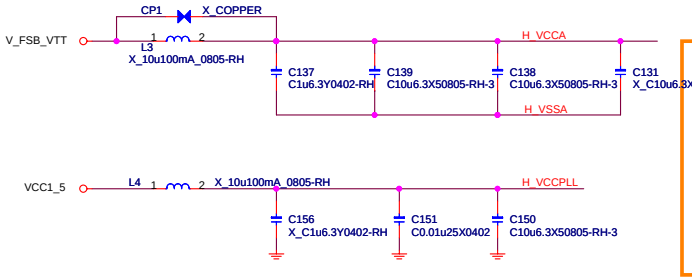
CPU LGA775 - Power



CPU GTLREF Voltage Should be 0.63 x VTT = 0.756V



*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE

VTT_OUT_LEFT	R198	X_130R1%0402	H_PROCHOT#	3,6
VTT_OUT_RIGHT	R133	62R0402	H_IERR#	3
	R131	62R0402	H_MERR#	3
V_FSB_VTT	R217	62R0402	H_CPURST#	3,6
VTT_OUT_LEFT	R160	150R1%0402	H_PWRGD	3,6
VTT_OUT_LEFT	R190	62R0402	H_BR#0	3,6

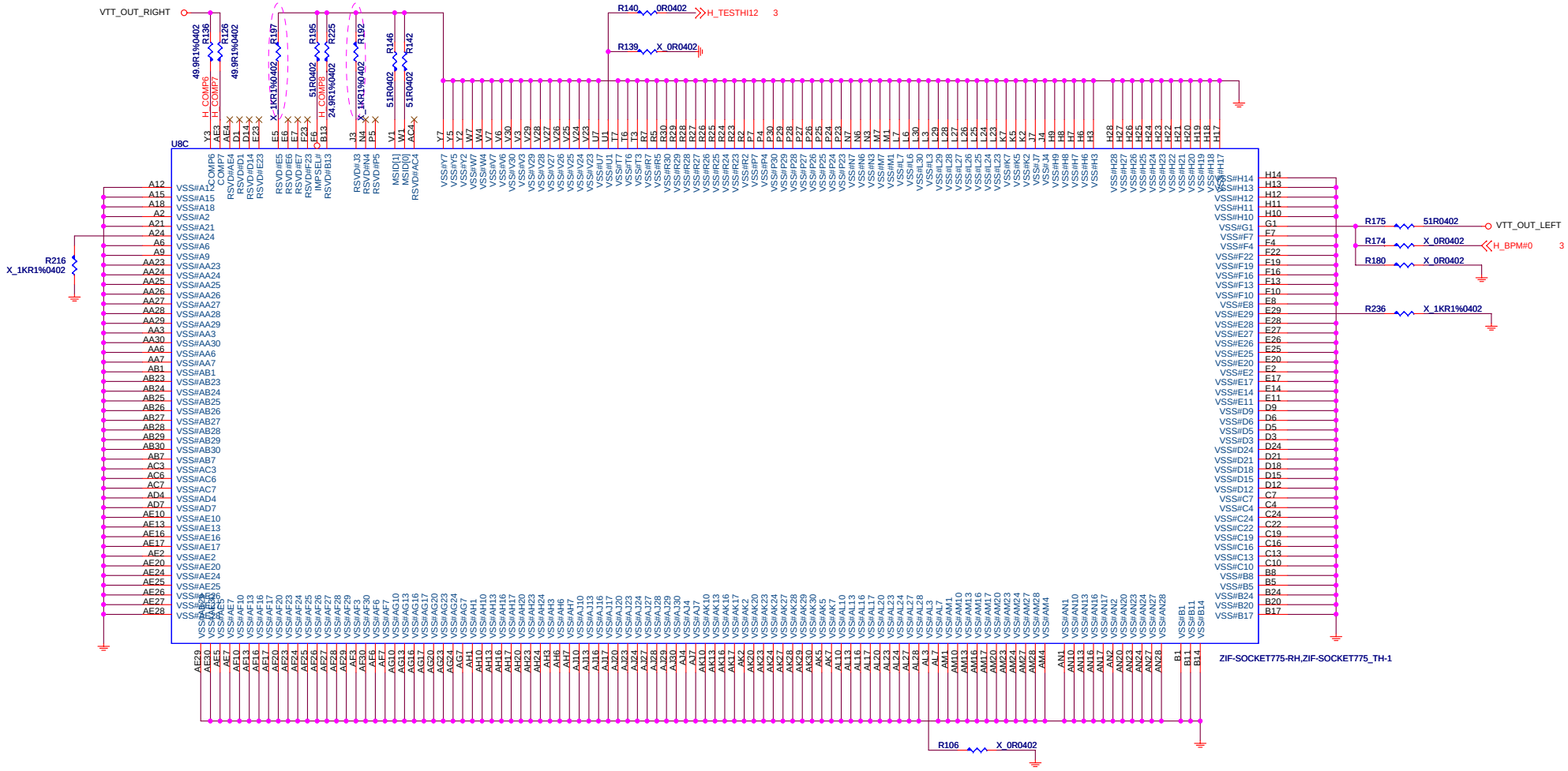
PLACE AT C55 END OF ROUTE

VTT_OUT_LEFT	R161	62R0402	TRMTRIP#	3,6
VTT_OUT_LEFT	R138	62R0402	H_FERR#	3,6

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	CPU LGA775 - Power	
Size	Document Number MS-7523	Rev 0A
Date: Friday, November 30, 2007	Sheet 4 of 38	

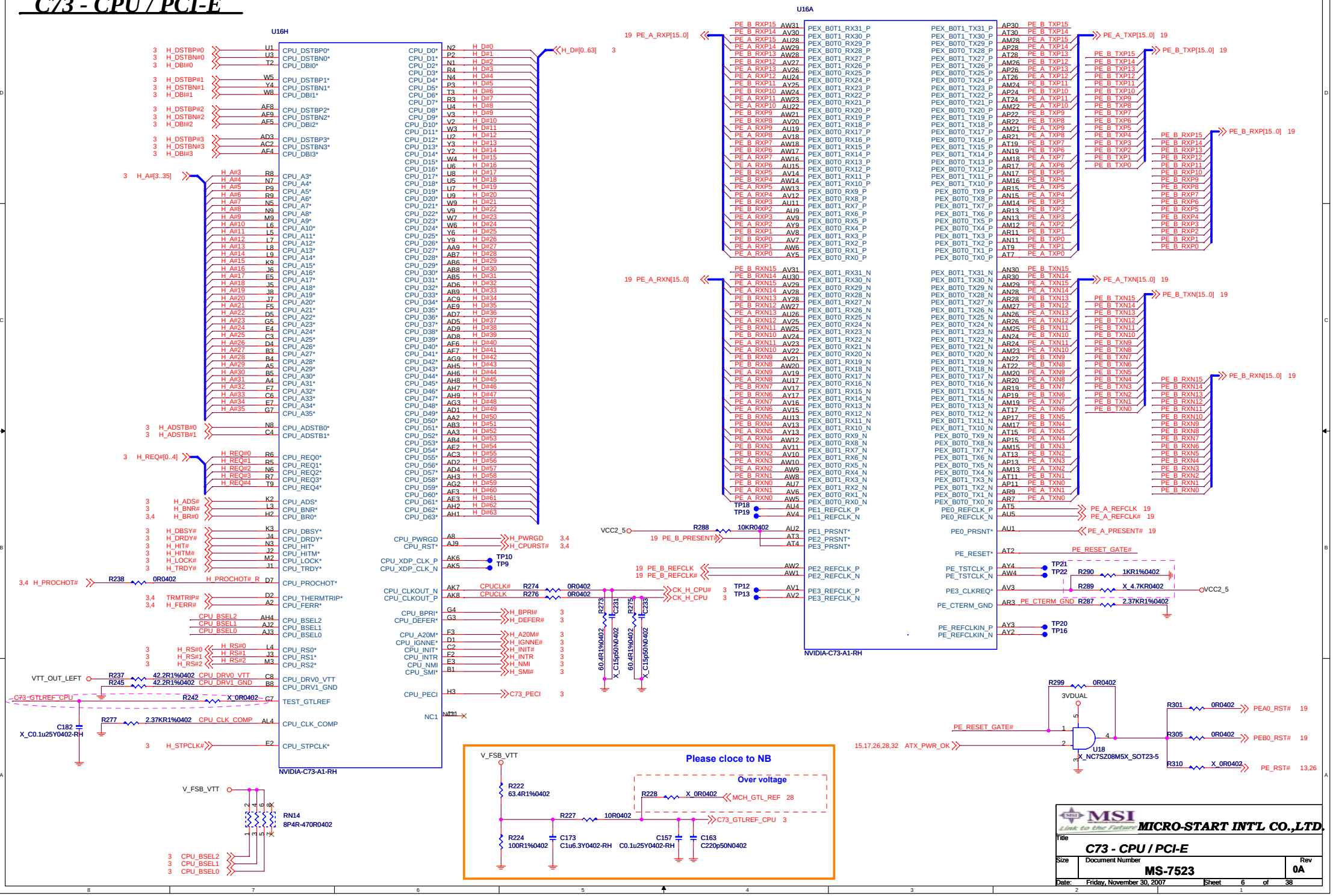
CPU LGA775 - Gnd



MICRO-START INT'L CO.,LTD.

Title	CPU LGA775 - Gnd	
Size	Document Number MS-7523	Rev 0A
Date: Friday, November 30, 2007	Sheet 5 of 38	

C73 - CPU / PCI-E


U16H
NVIDIA-C73-A1-RH
U16A
NVIDIA-C73-A1-RH
Please cloce to NB
Over voltage
RN14
8P4R-470R0402
MICRO-START INT'L CO.,LTD.
C73 - CPU / PCI-E
MS-7523
0A
Friday, November 30, 2007
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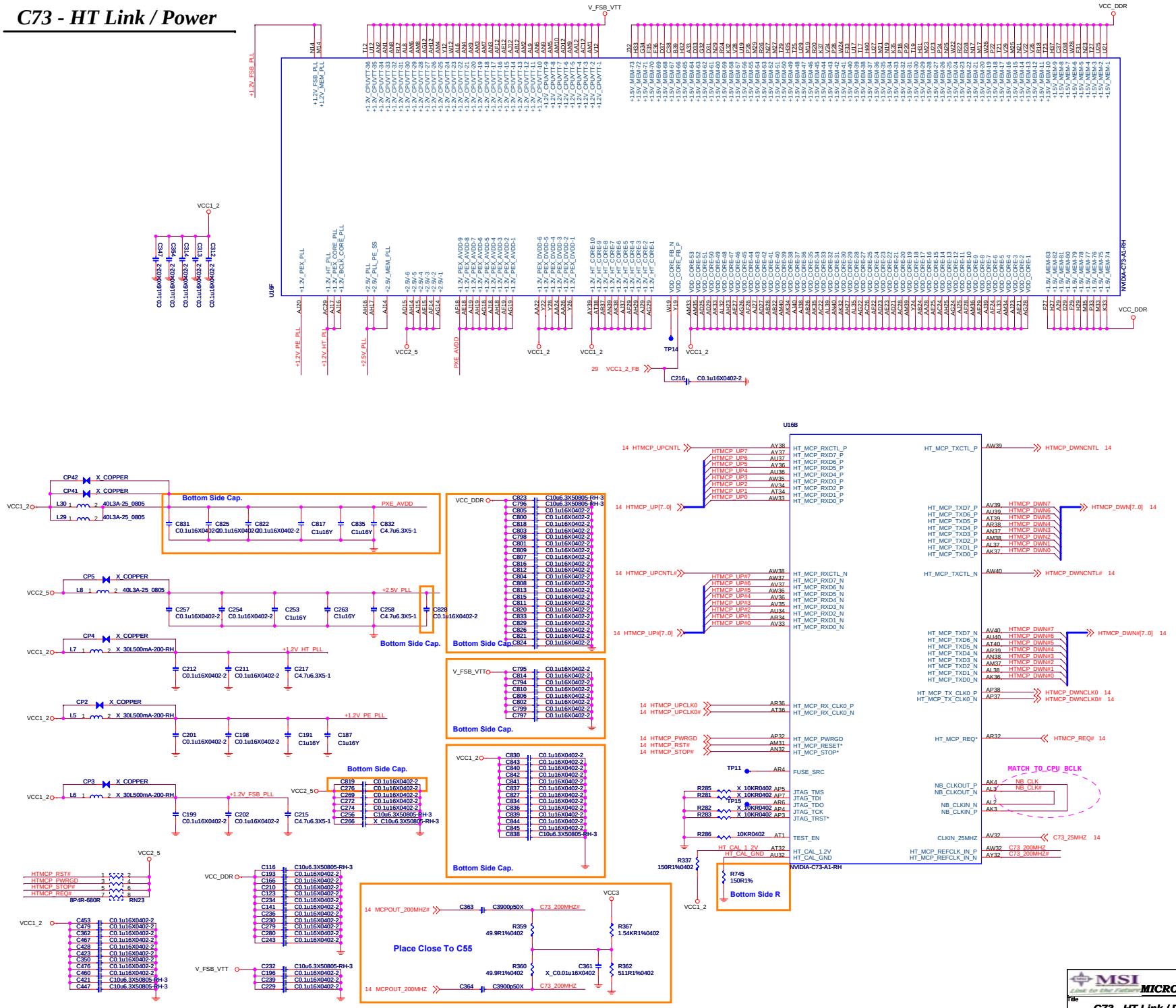
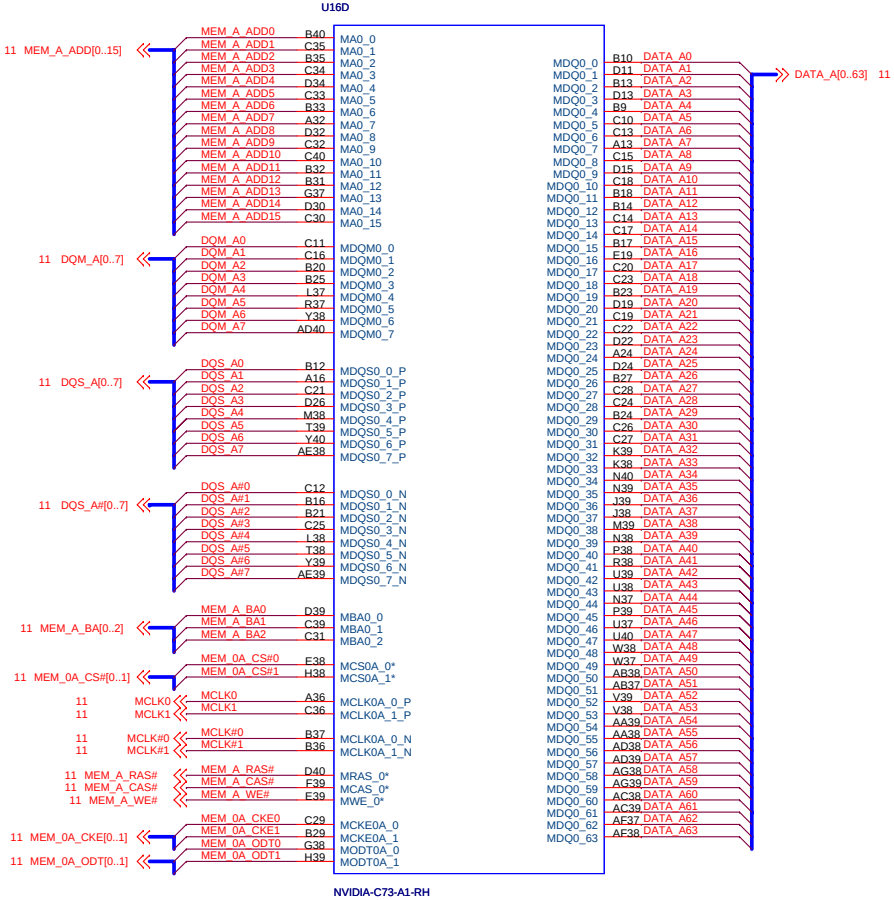
C73 - HT Link / Power



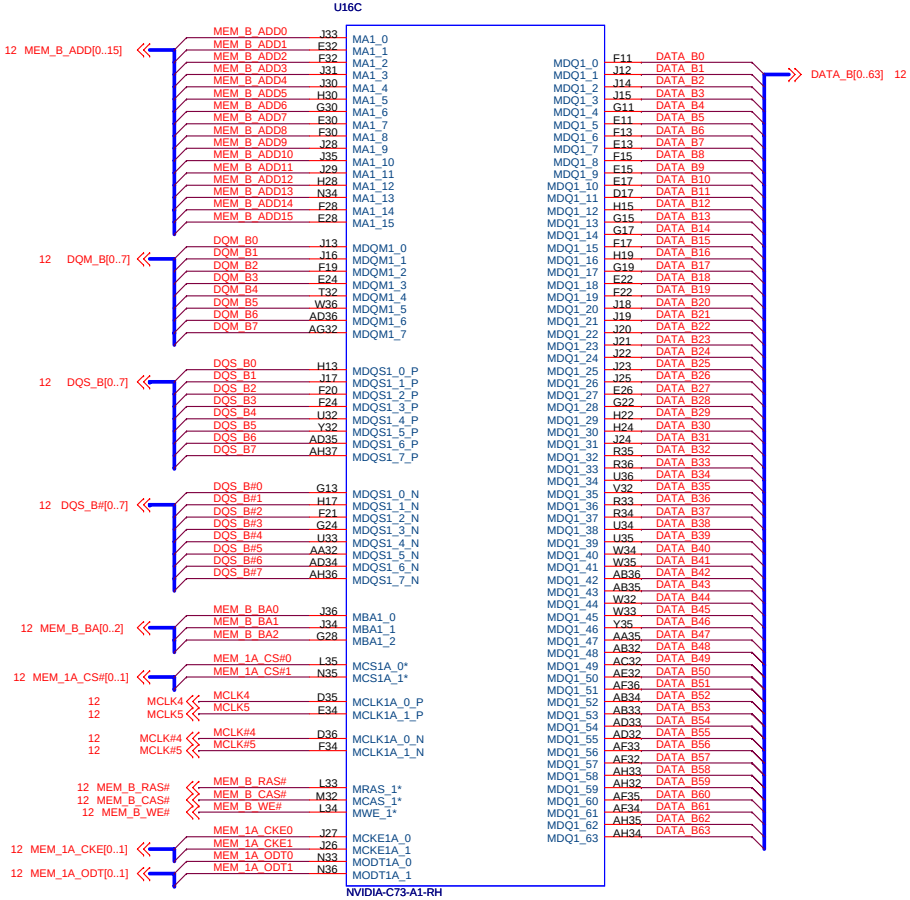
MSI Link to the Future	MICRO-START INT'L CO.,LTD.
Title	C73 - HT Link / Power
Size	Document Number: MS-7523
Rev	0A
Date: Friday, November 30, 2007	Sheet 7 of 38

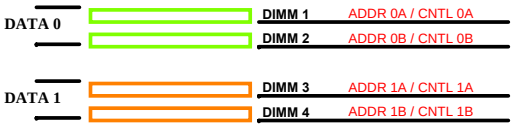
C73 - Memory A0

DIMM1 0A



DIMM3 1A



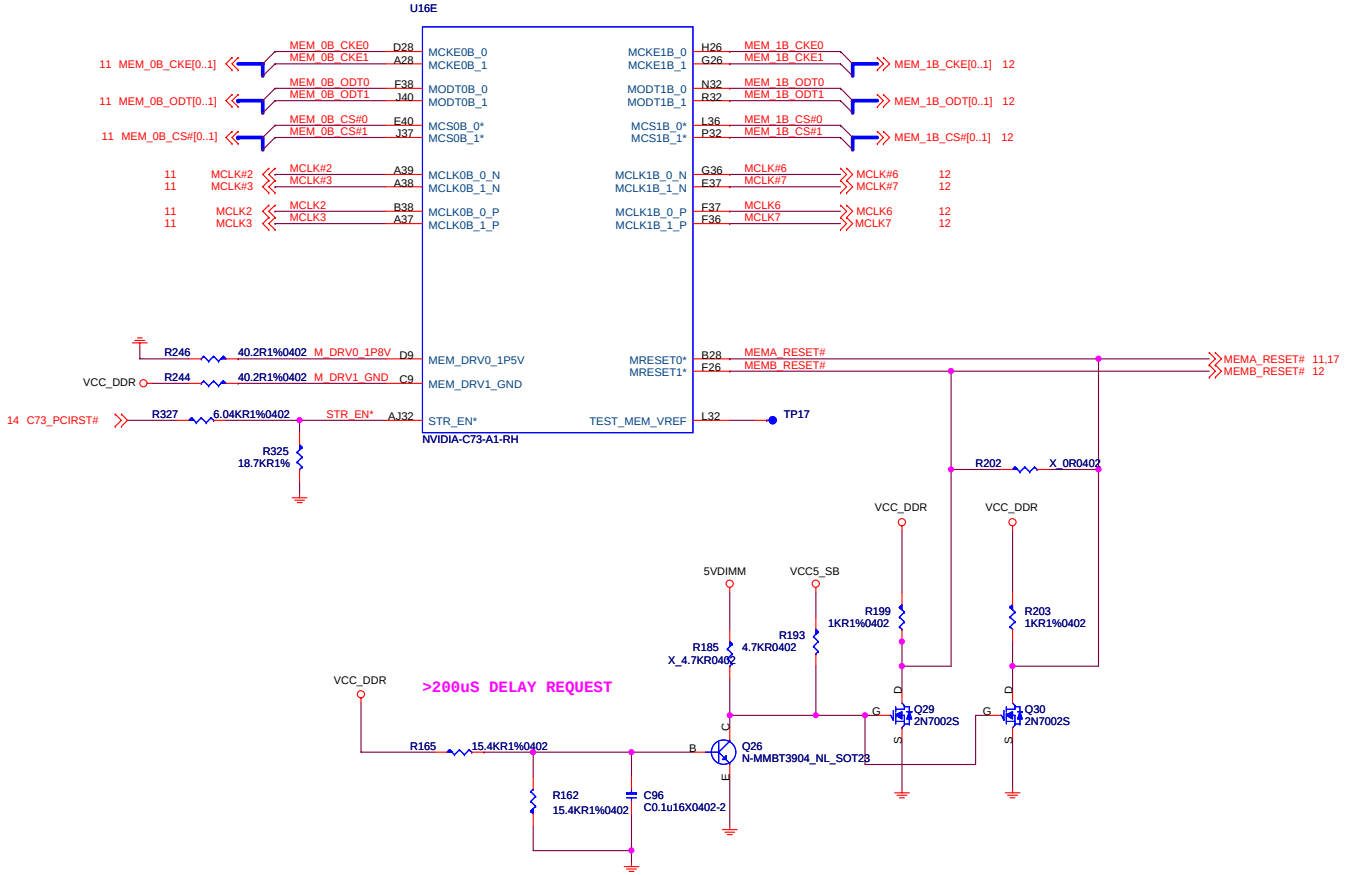


MICRO-START INT'L CO.,LTD.

Title		
C73 - Memory A0		
Size	Document Number MS-7523	Rev 0A
Date: Friday, November 30, 2007	Sheet 8 of 38	

C73 - Memory A1

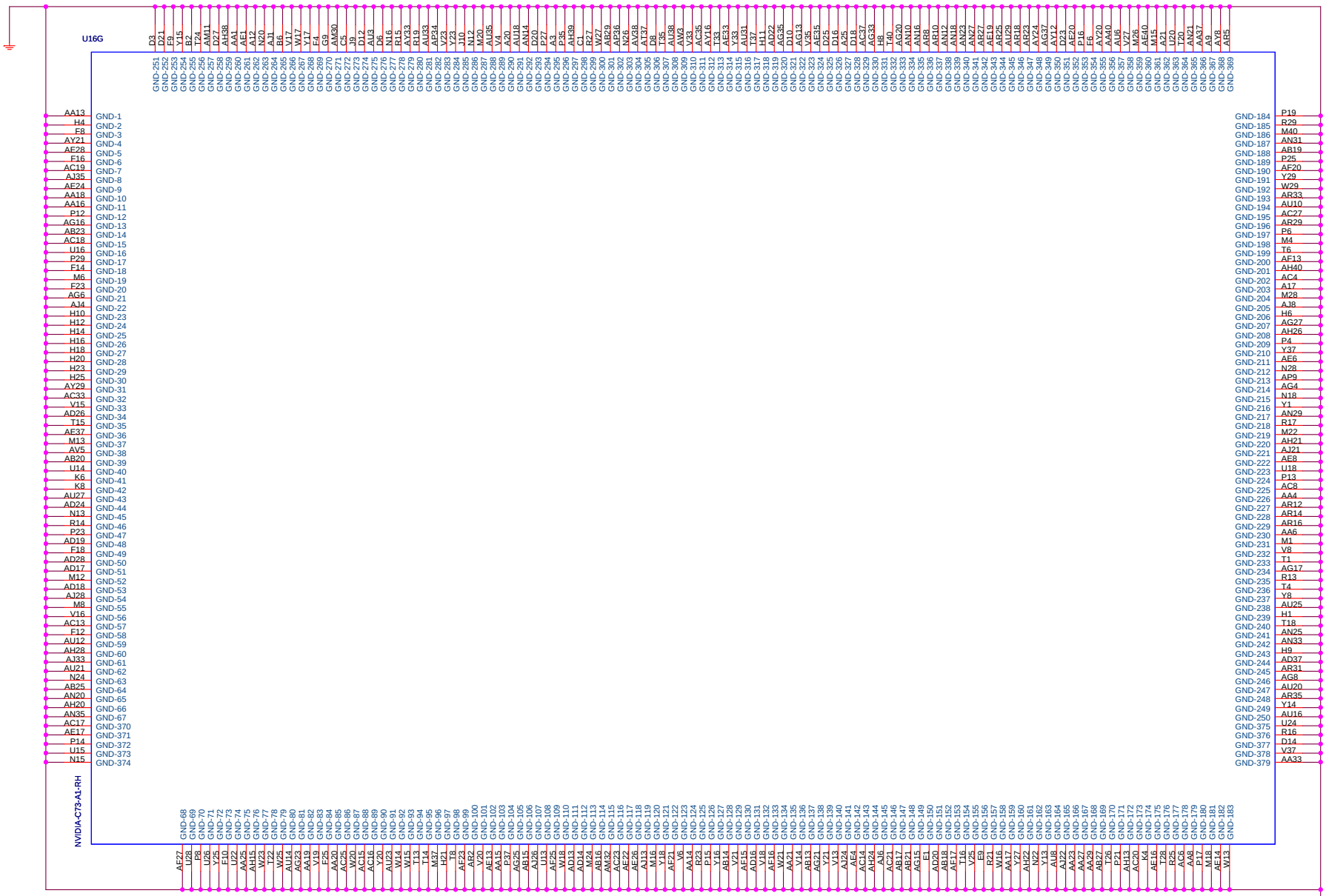
DIMM2 0B /DIMM4 1B



MICRO-START INT'L CO.,LTD.

Title		
	C73 - Memory A1	
Size	Document Number MS-7523	Rev 0A
Date: Friday, November 30, 2007	Sheet 9 of 38	

C73 - Gnd

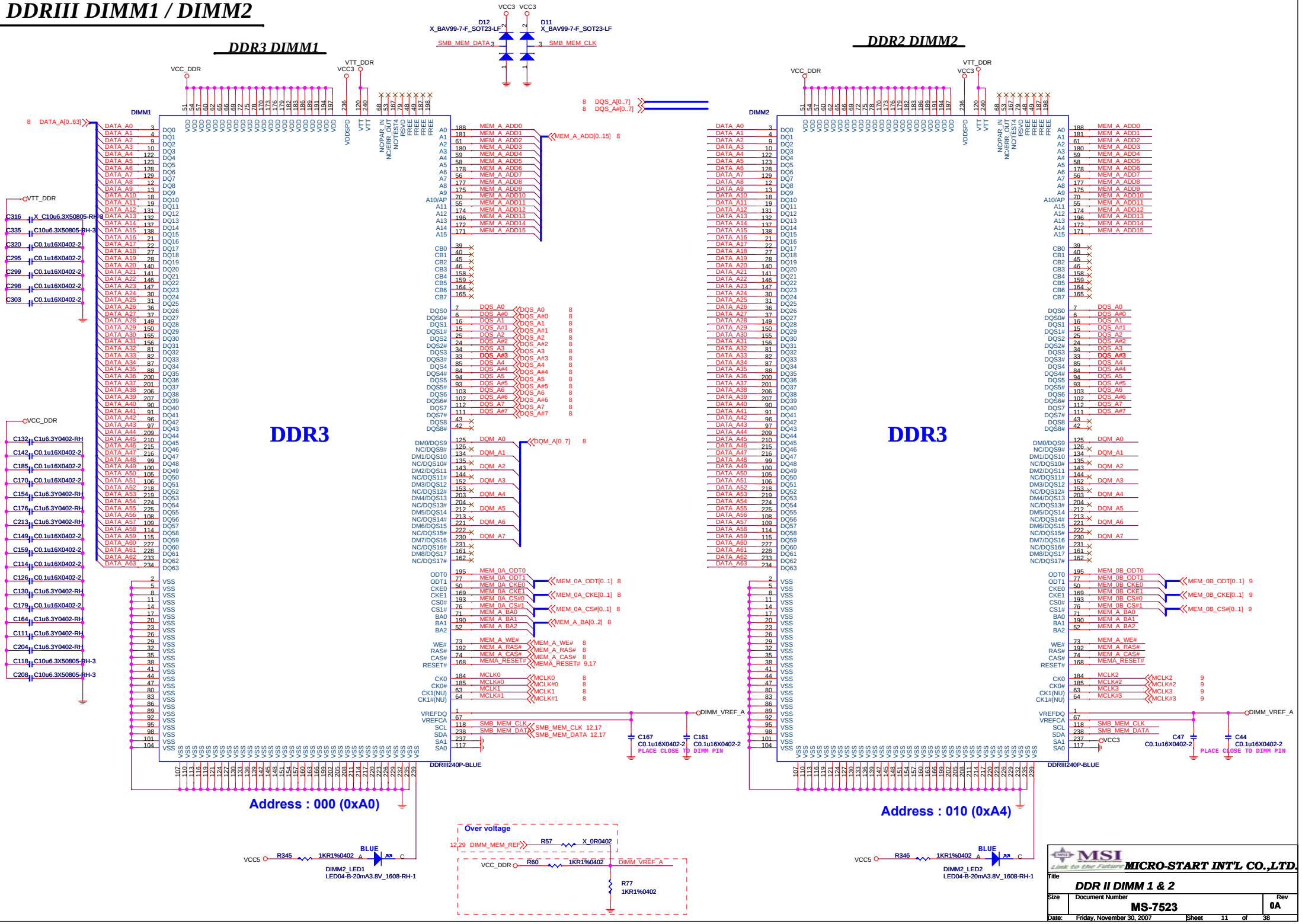


Title	Document Number	Rev
C73 - Gnd	MS-7523	0A

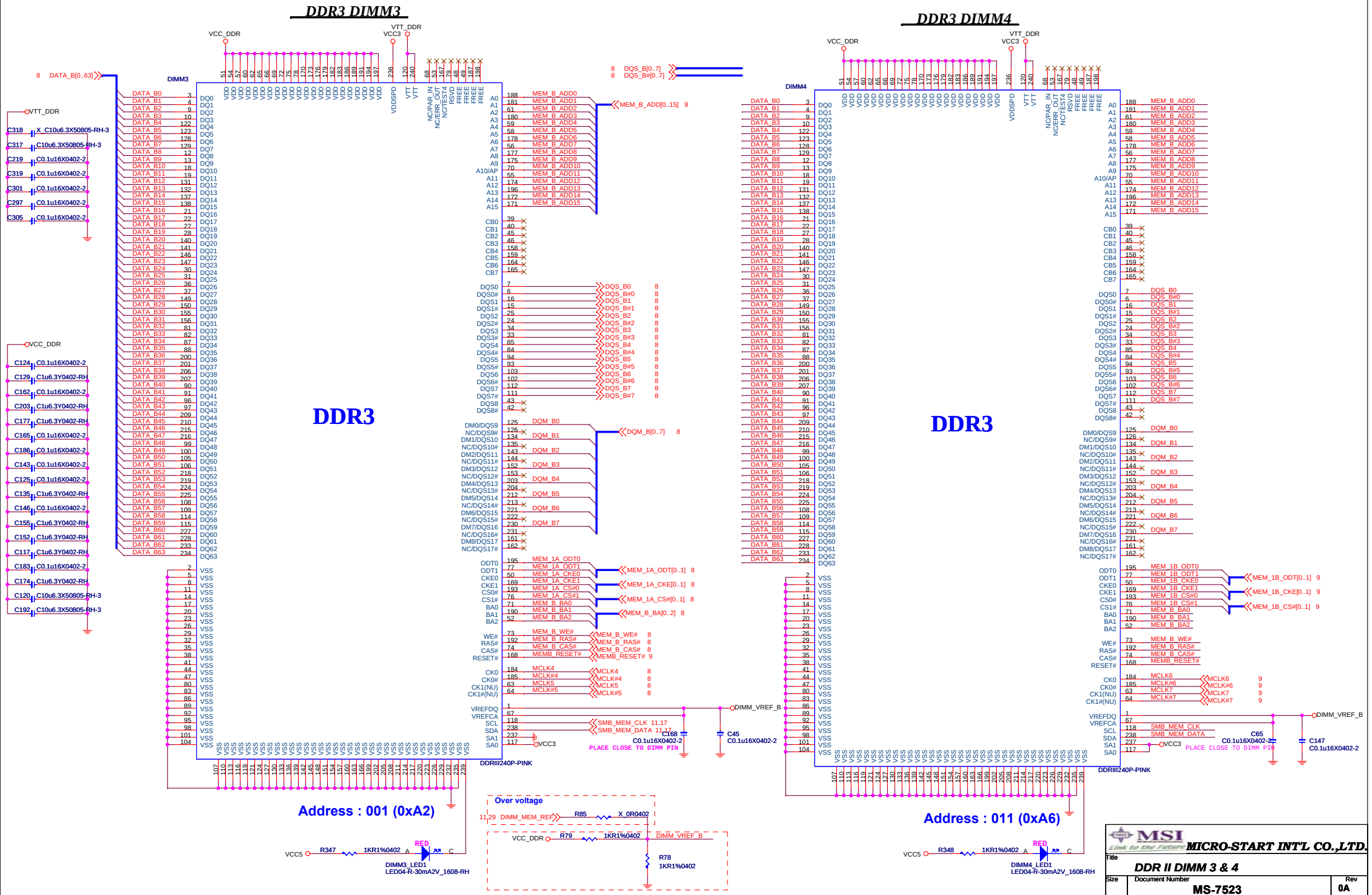
MICRO-START INT'L CO.,LTD.

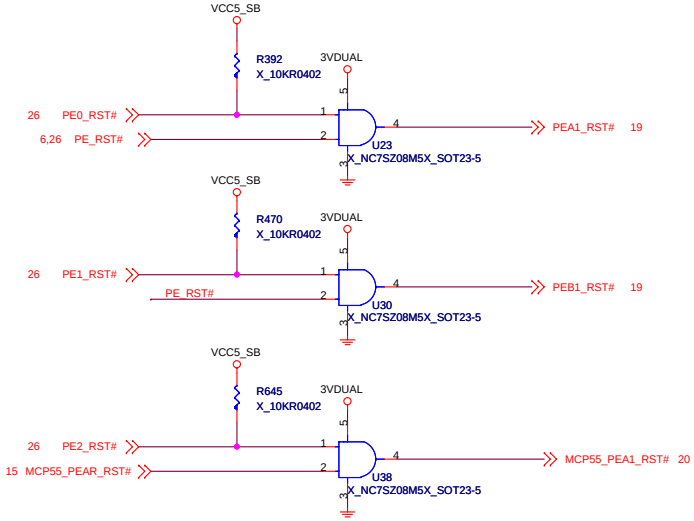
Size | Date: Friday, November 30, 2007 | Sheet 10 of 38

DDRIII DIMM1 / DIMM2

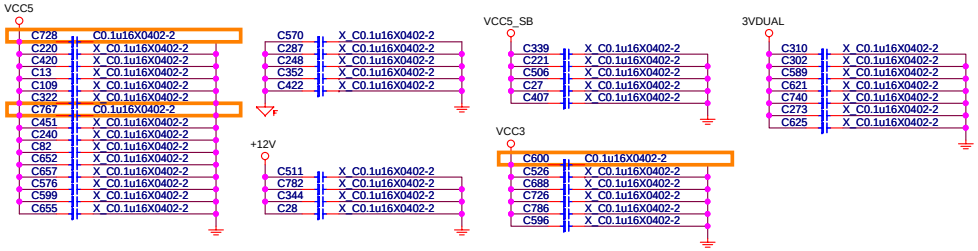


DDRII DIMM3 / DIMM4





EMI Solution 2007-10-25



MICRO-START INT'L CO.,LTD.

Title		
PCIE RESET		
Size	Document Number	Rev
	MS-7523	0A

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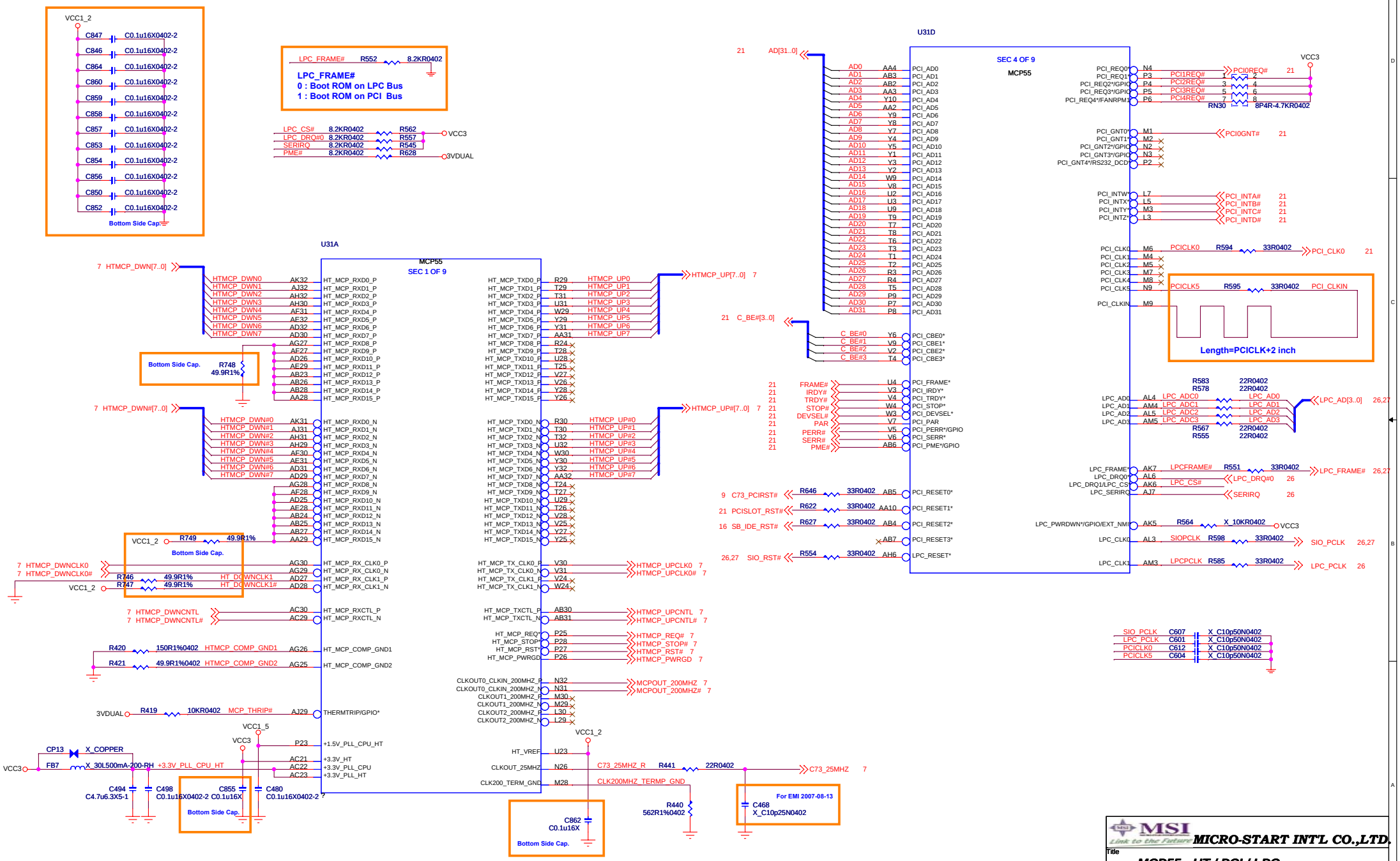
MCP55 - HT / PCI / LPC



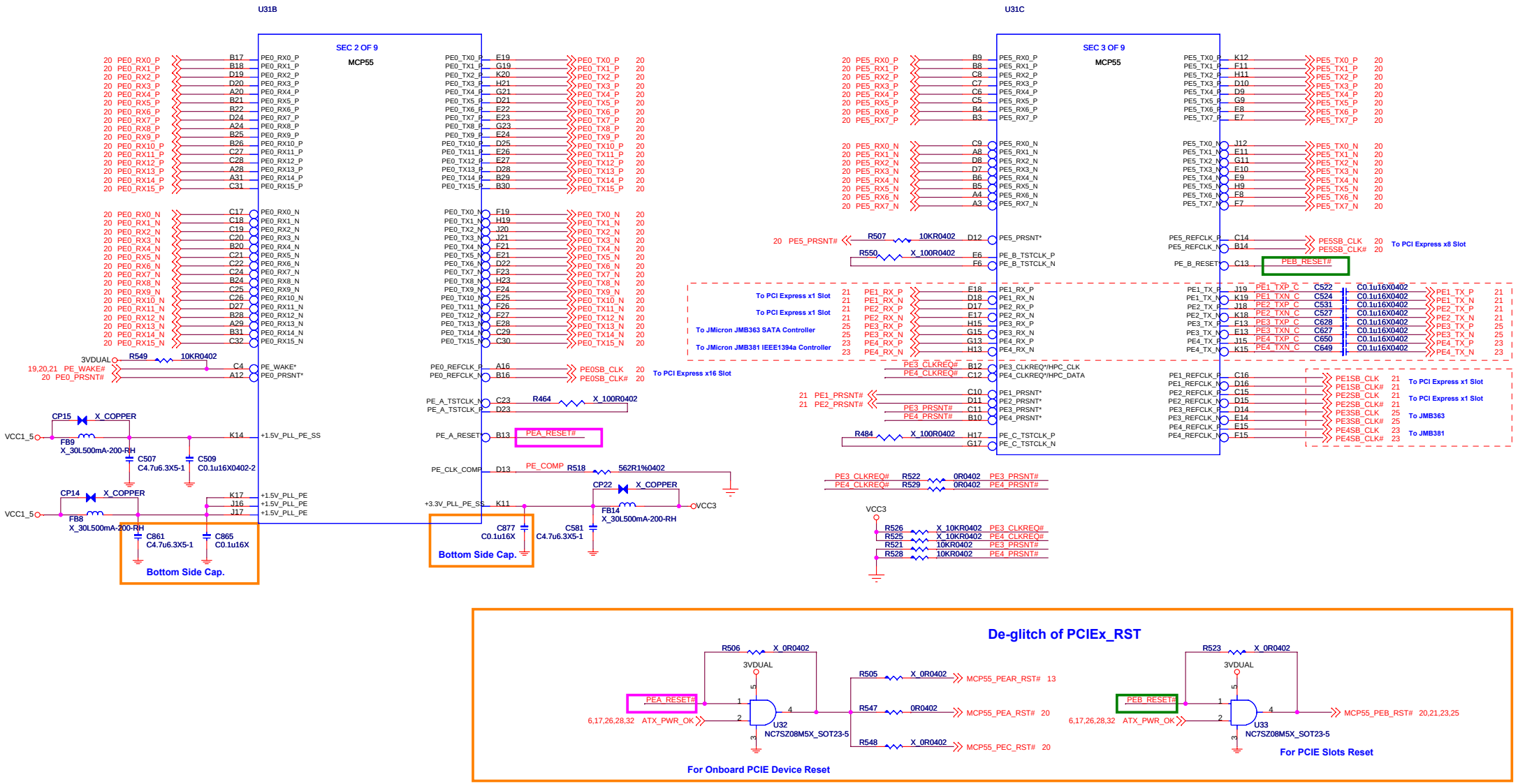
MICRO-START INT'L CO.,LTD.

Title: MCP55 - HT / PCI / LPC

Size	Document Number	Rev
	MS-7523	0A

Date: Friday, November 30, 2007 Sheet 14 of 38

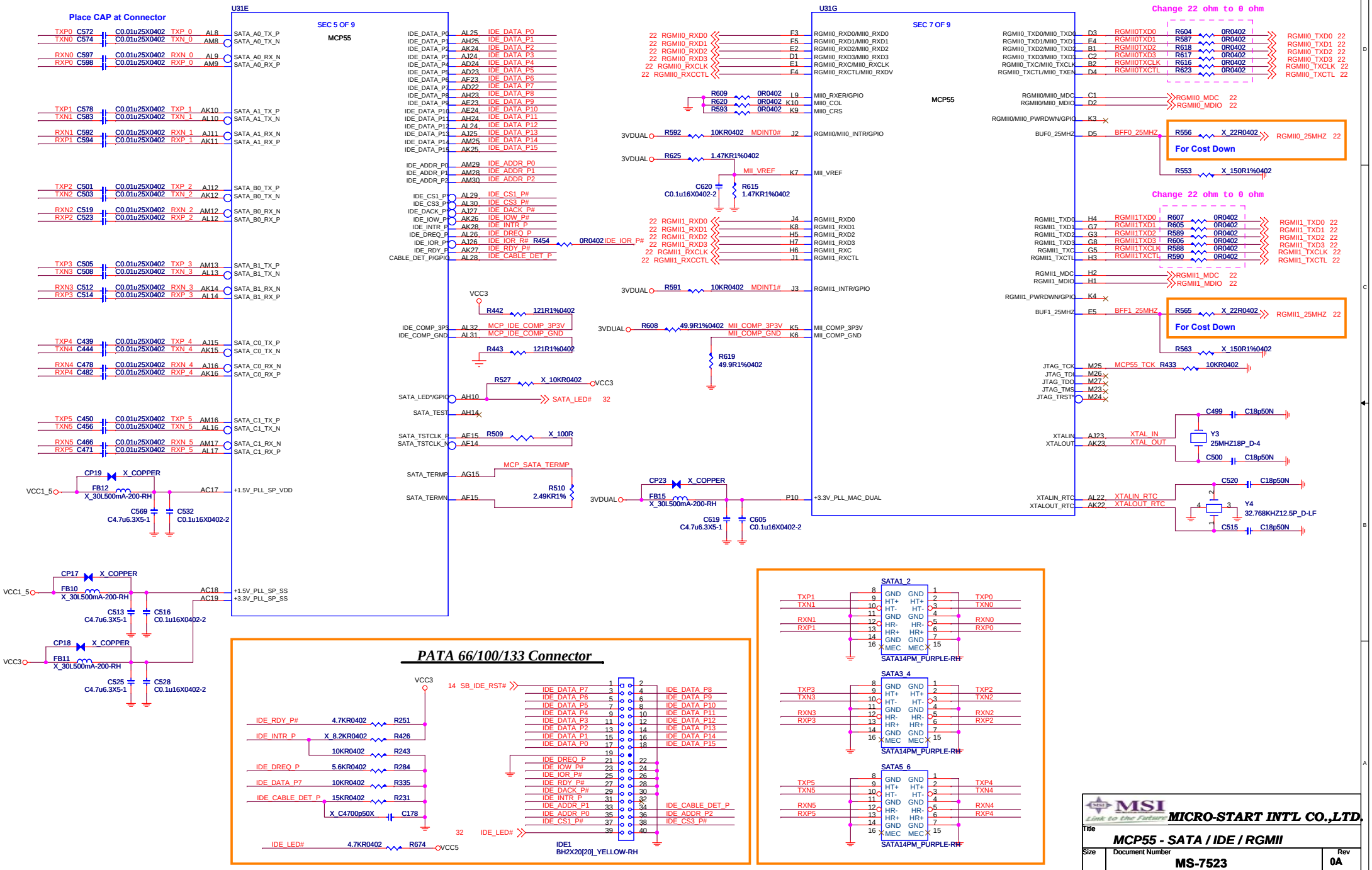
MCP55 - PCI-E



MICRO-START INT'L CO.,LTD.

Title		
MCP55 - PCI-E		
Size	Document Number	Rev
	MS-7523	0A
Date: Friday, November 30, 2007	Sheet 15 of 38	

MCP55 - SATA / IDE / RGMII



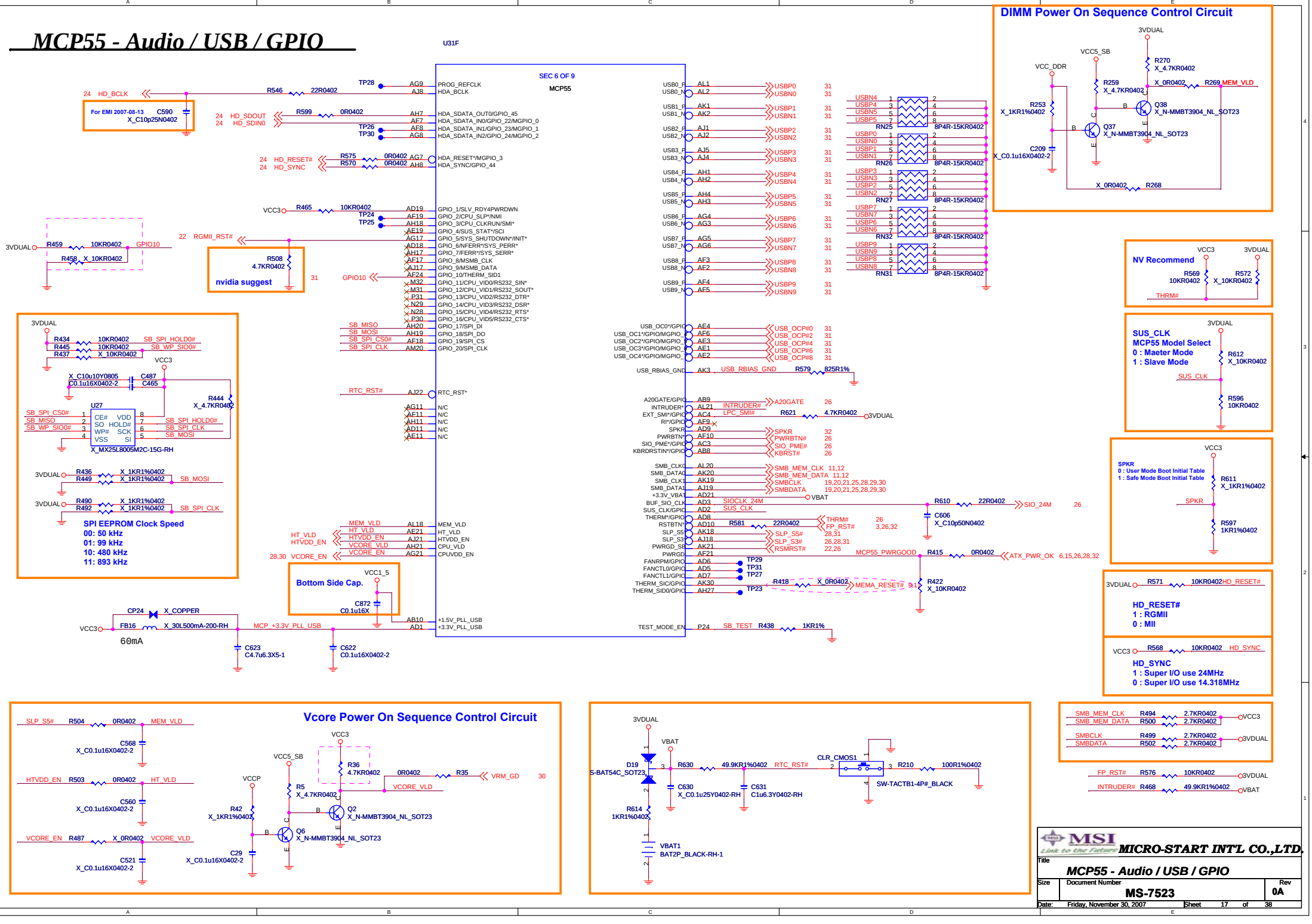
MICRO-START INT'L CO.,LTD.

Title: MCP55 - SATA / IDE / RGMII

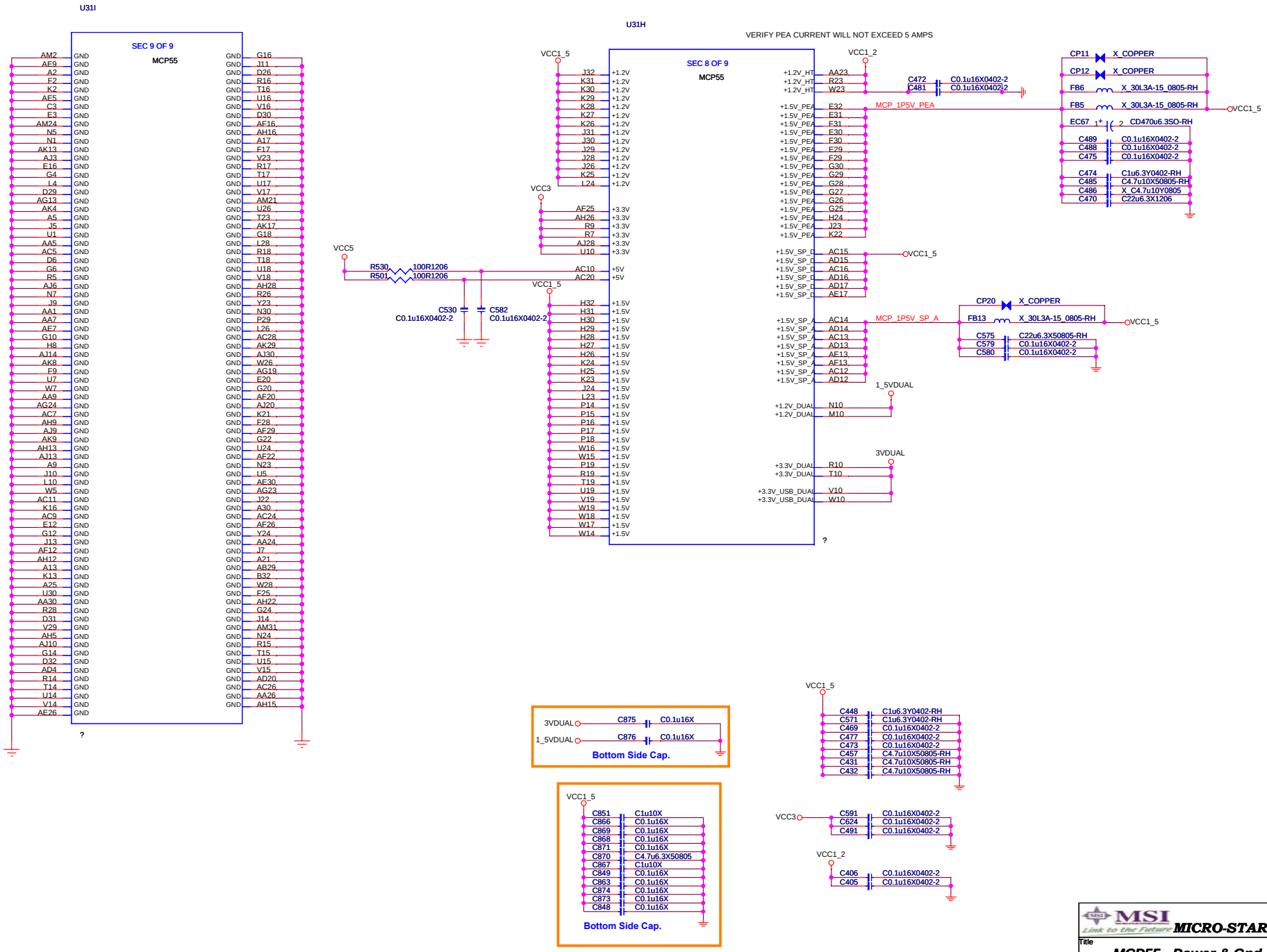
Size | Document Number: MS-7523 | Rev: 0A

Date: Friday, November 30, 2007 | Sheet 16 of 38

MCP55 - Audio / USB / GPIO



MCP55 - Power & Gnd



MICRO-START INT'L CO.,LTD.

Title	MCP55 - Power & Gnd	
Size	Document Number MS-7523	Rev 0A
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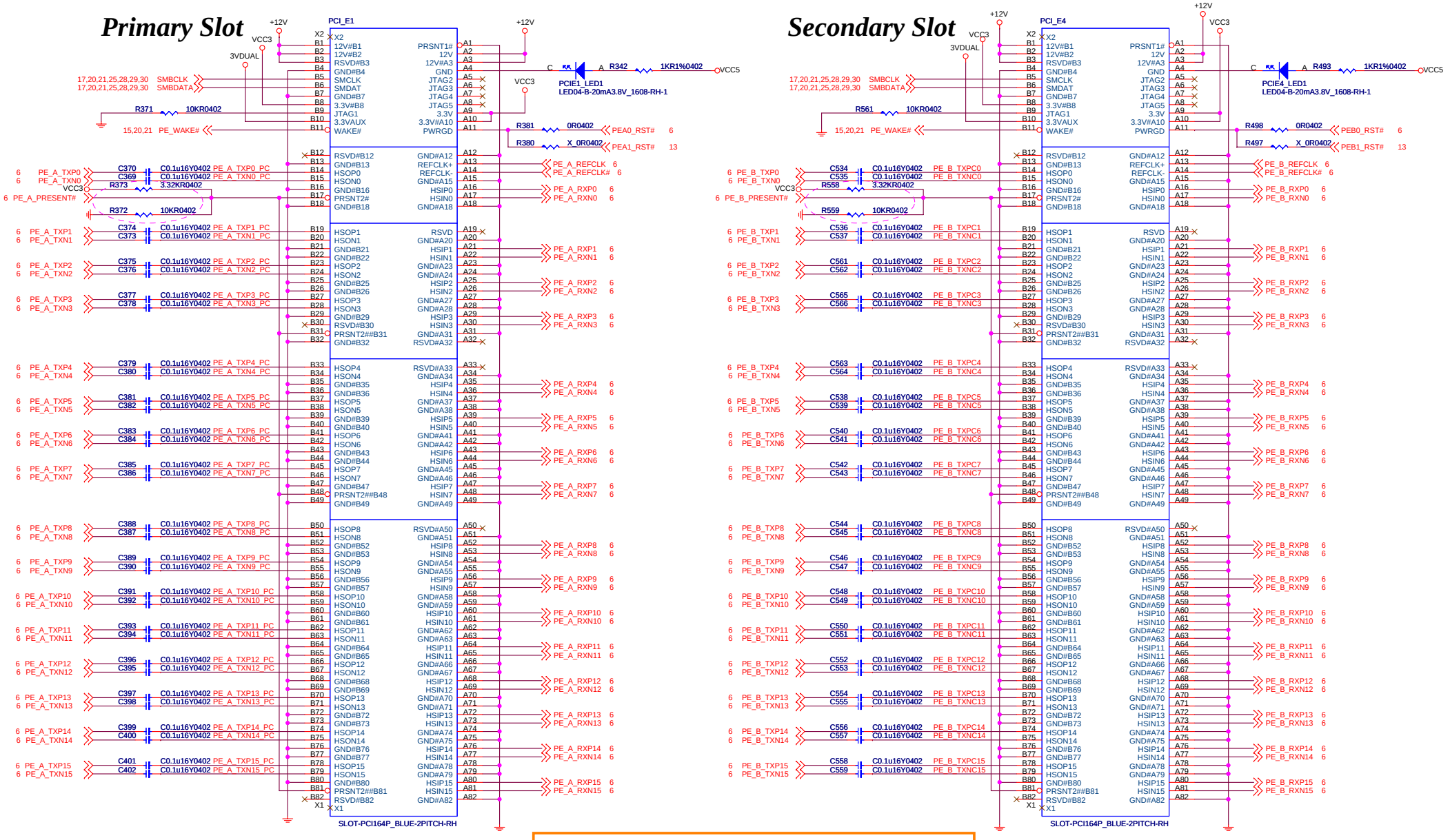
PCI-Express x16 Primary and Secondary Slot



MICRO-START INT'L CO.,LTD.

Title: NB PCI-E x16 Pri / Sec Slot

Size	Document Number	Rev
	MS-7523	0A

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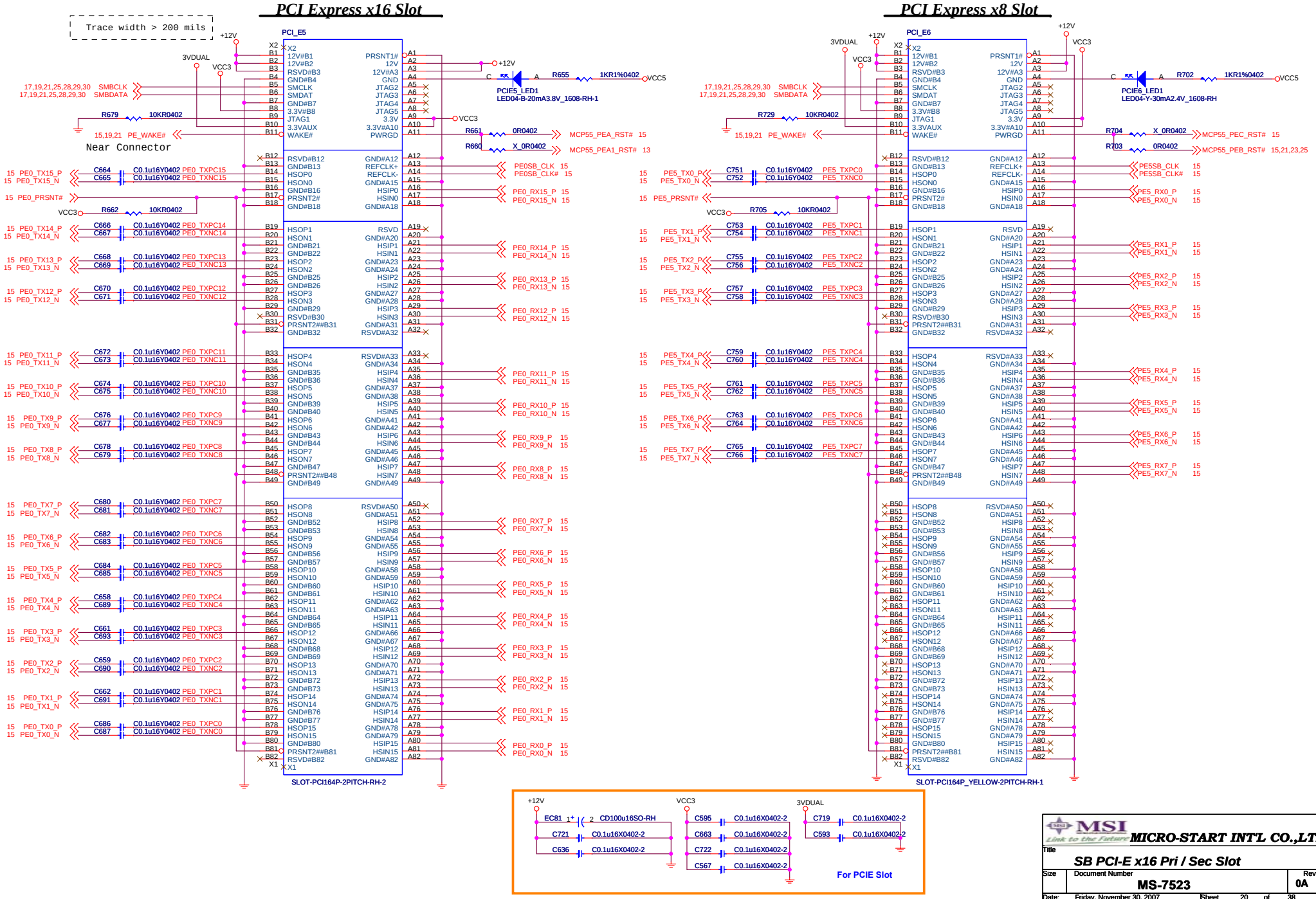
SB PCI Express x16 Slot and PCI Express x8 Slot



MICRO-START INT'L CO.,LTD.

Title: SB PCI-E x16 Pri / Sec Slot

Size | Document Number: MS-7523 | Rev: 0A

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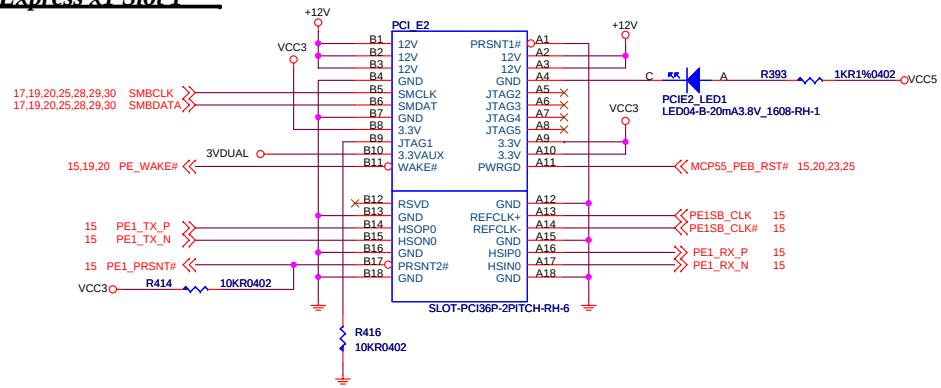
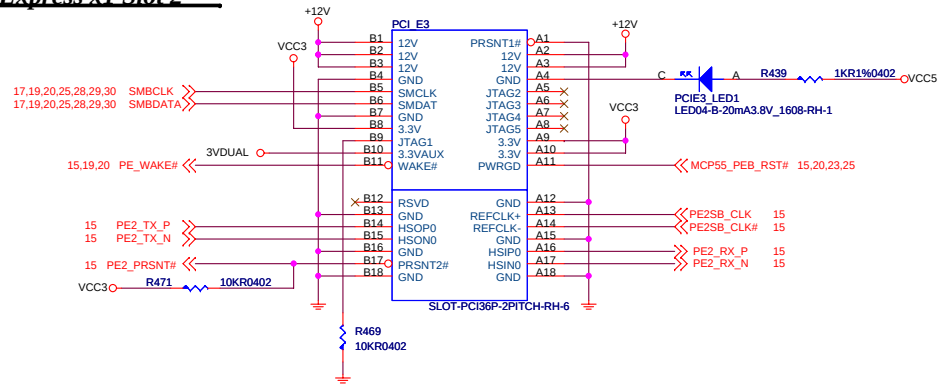
SB PCI-Express x1 Slots and PCI Slot

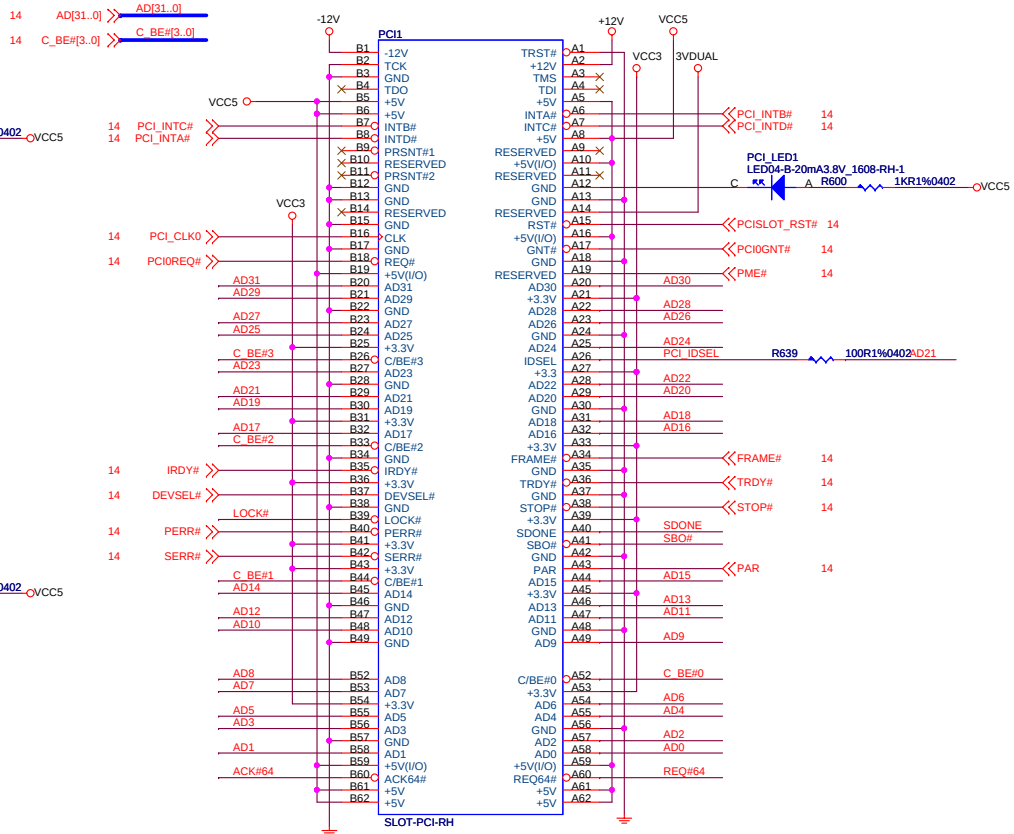
PCI Express x1 Slot 1



PCI Express x1 Slot 2

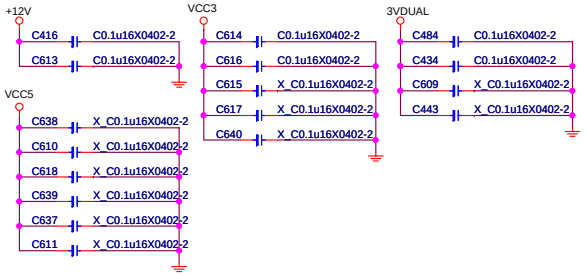


PCI Slot 1 (PCI VER: 2.2 Comply)

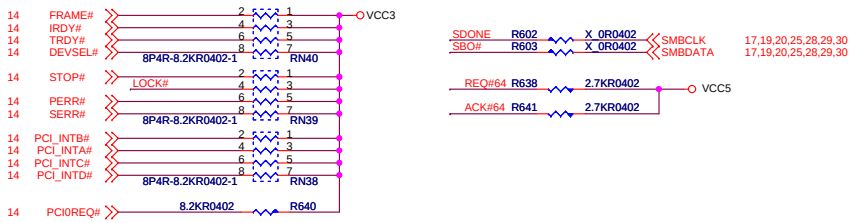


IDSEL = AD21
MASTER = PCI0REQ#
PCI0GNT*

PCI Slot Decoupling Capacitors



PCI Pull Up / Down Resistors



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title		
SB PCI-E x1 / PCI Slot		
Size	Document Number **MS-7523**	Rev **0A**
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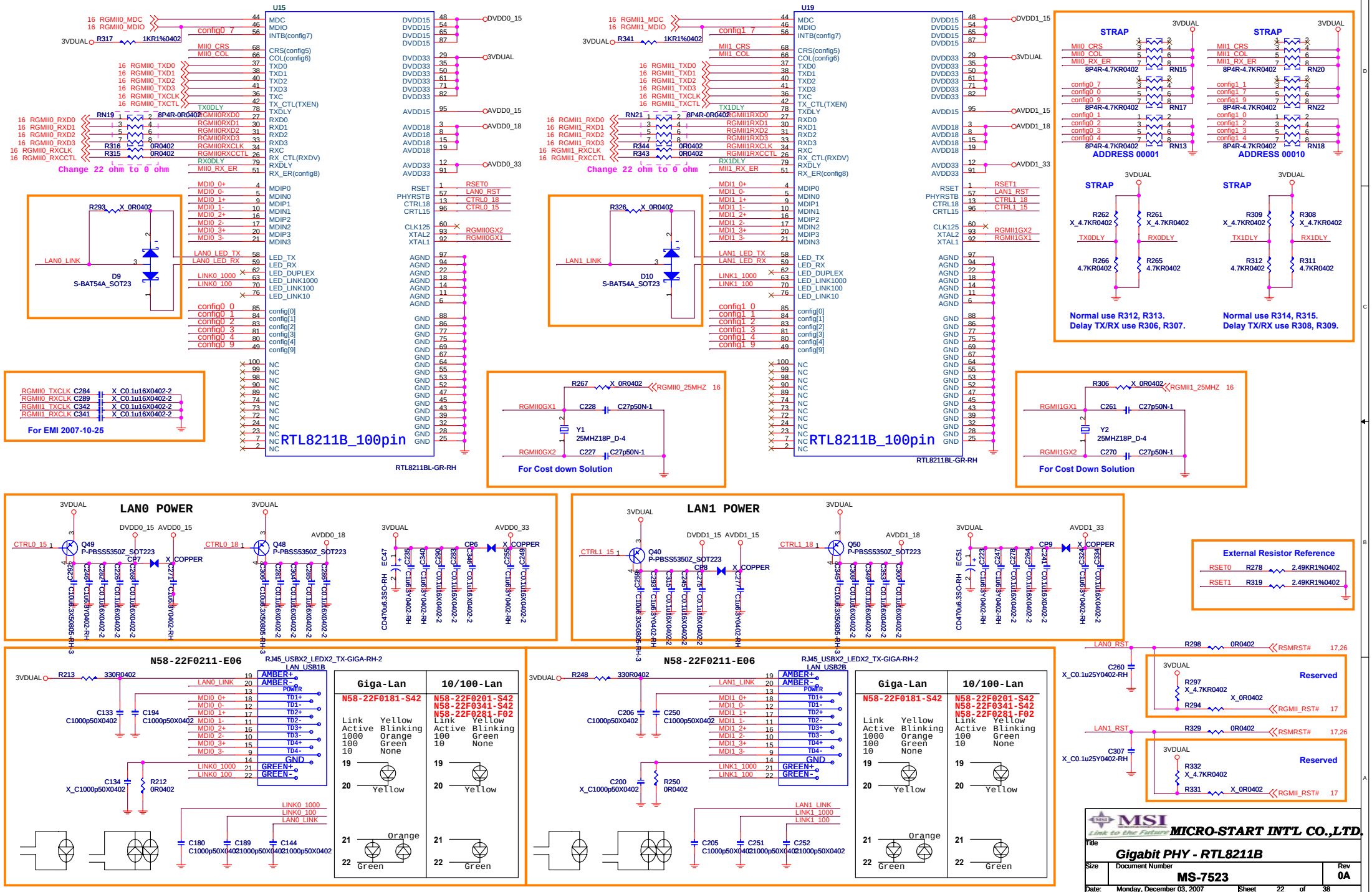
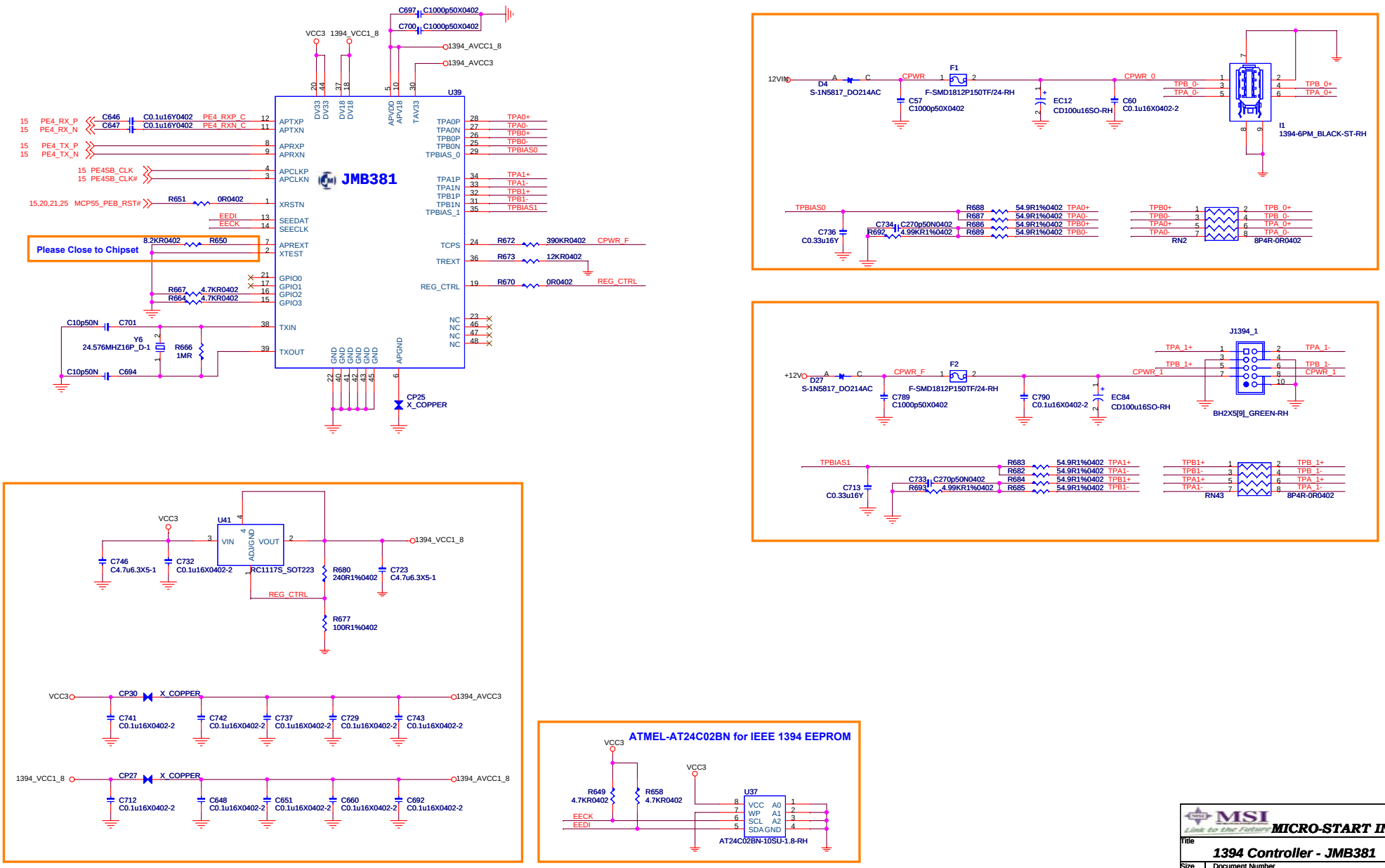
RTL8211B RGMII Gigabit PHY (Lan 1 and Lan 2)



PCIE To 1394a OHCI Host Controller - JMB381



MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title	1394 Controller - JMB381	
Size	Document Number MS-7523	Rev 0A
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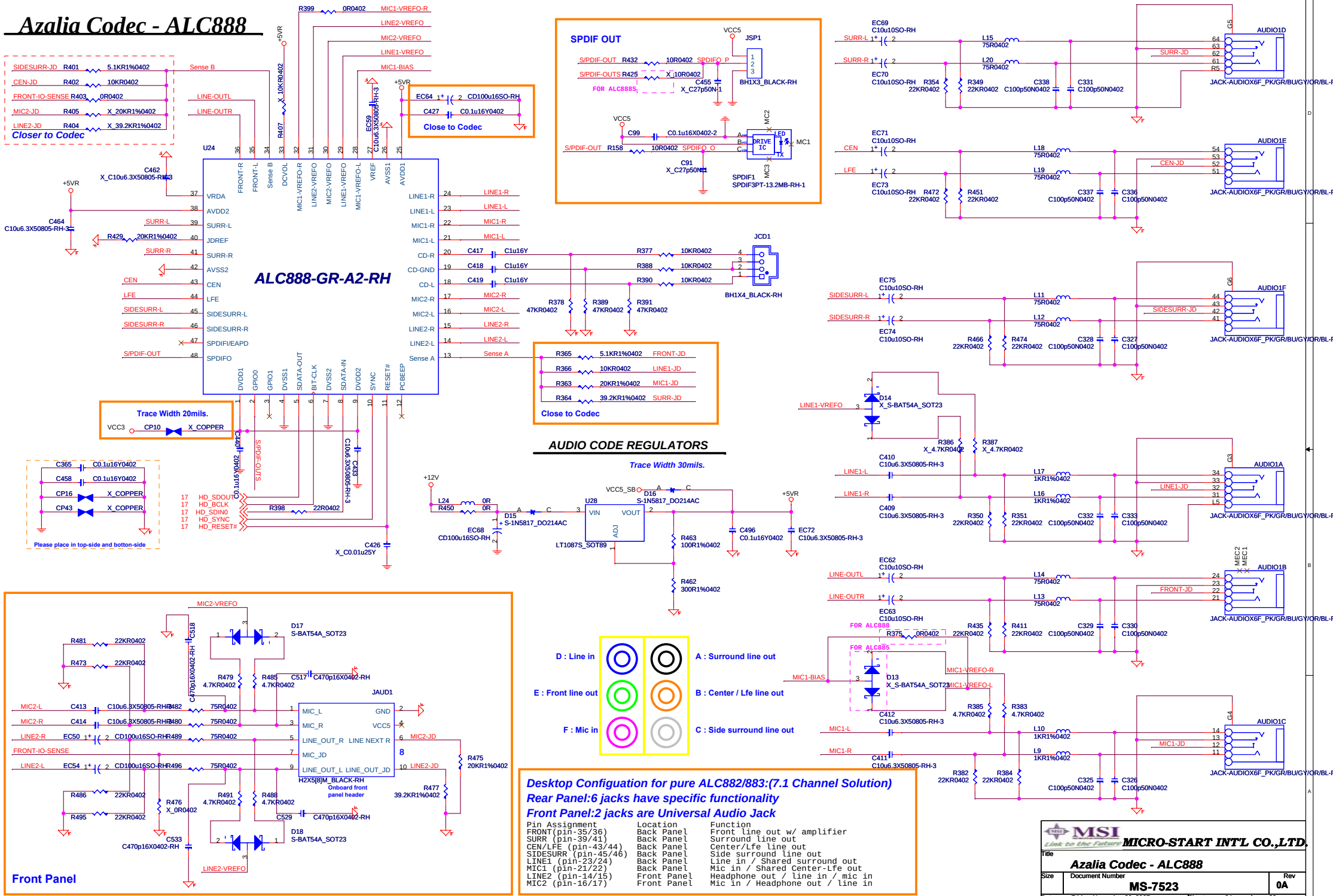
Azalia Codec - ALC888



Desktop Configuation for pure ALC882/883:(7.1 Channel Solution)

Rear Panel:6 jacks have specific functionality

Front Panel:2 jacks are Universal Audio Jack

Pin Assignment	Location	Function
FRONT(pin-35/36)	Back Panel	Front line out w/ amplifier
SURR (pin-39/41)	Back Panel	Surround line out
CEN/LFE (pin-43/44)	Back Panel	Center/Lfe line out
SIDESURR (pin-45/46)	Back Panel	Side surround line out
LINE1 (pin-23/24)	Back Panel	Line in / Shared surround out
MIC1 (pin-21/22)	Back Panel	Mic in / Shared Center-Lfe out
LINE2 (pin-14/15)	Front Panel	Headphone out / line in / mic in
MIC2 (pin-16/17)	Front Panel	Mic in / Headphone out / line in

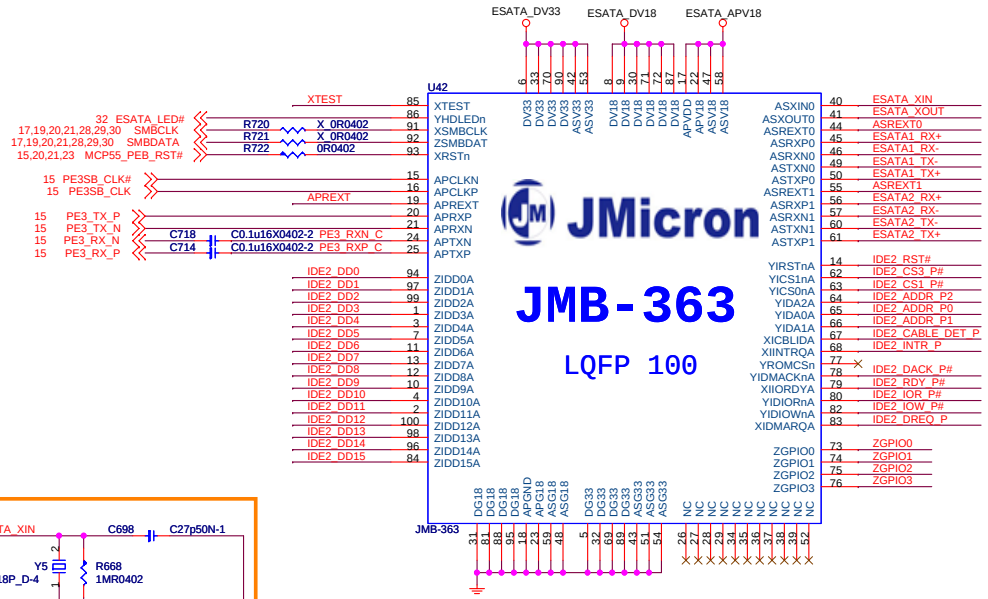
MSI Link to the Future MICRO-START INT'L CO.,LTD.

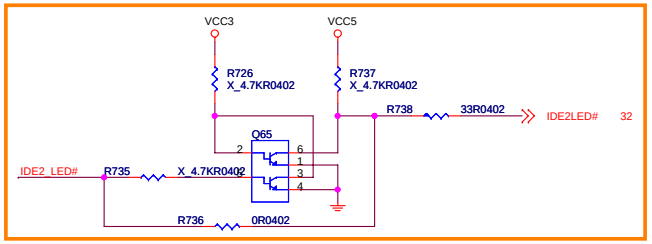
Title: Azalia Codec - ALC888

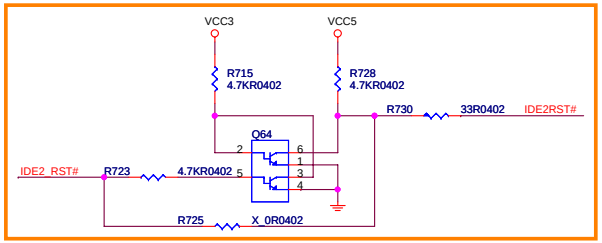
Size | Document Number: MS-7523 | Rev: 0A

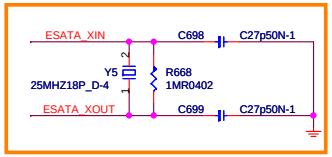
Date: Friday, November 30, 2007 | Sheet 24 of 38

JMicron JMB363 eSATA Controller





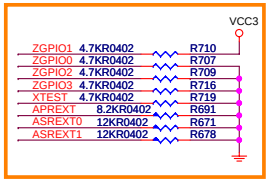


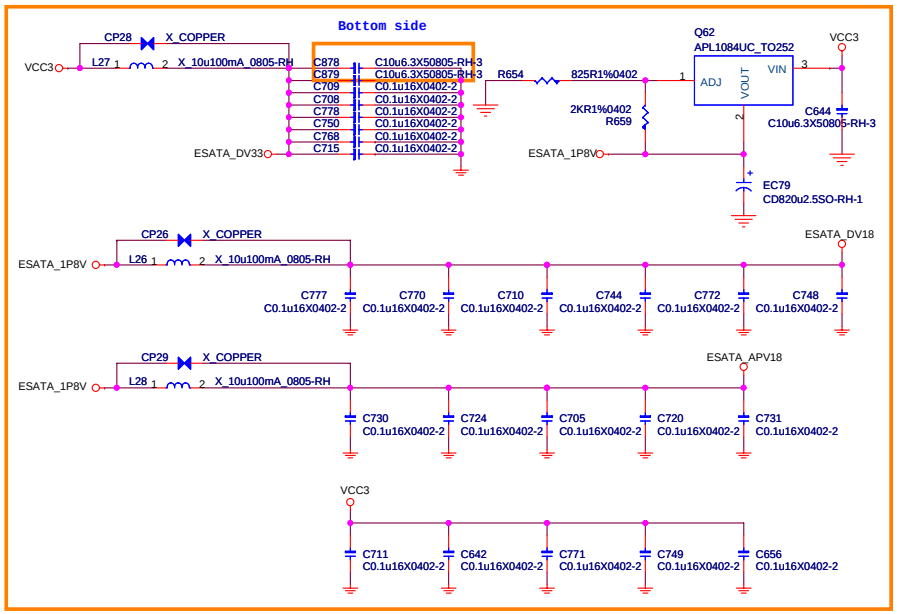


SATA II Port 0 External Reference Resistor.
An external 12KΩ±1%resistor should be connected and bypass to the ground ASG18 (pin#48).

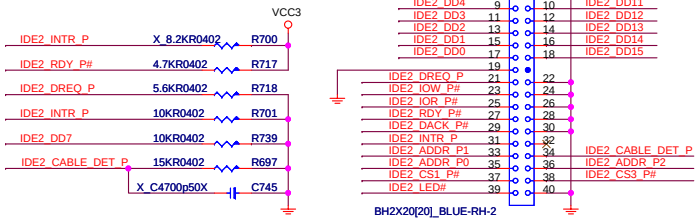
SATA II Port 0 External Reference Resistor.
An external 12KΩ±1%resistor should be connected and bypass to the ground ASG18 (pin#59).

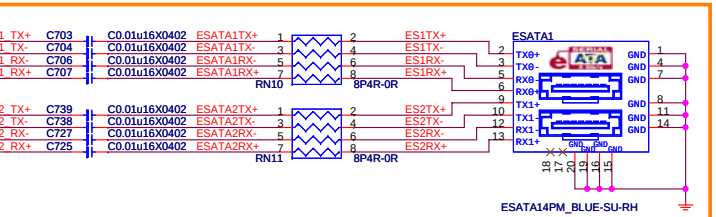
PCI Express External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground APG18 (pin#18).





PATA 66/100/133 Connector





JMB363 GPIO0
It uses to control function# available on JMB363.
0: single function ; 1: multi-function
JMB363 GPIO1
It uses to control clock source of SATA II port 0.
0: from internal clock source from PCI Express clock source
1: from ASXIN0 & ASXOUT0
JMB363 GPIO2
It uses to control interface to access internal debug registers.
0: SMBus I/F ; 1: Reserved for debugging.
JMB363 GPIO3
Reserved for debugging.
JMB363 Test Mode Enable.
High-active signal to enable testing and debug modes of JMB363.

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Title	JMicron JMB363 eSATA Controller	
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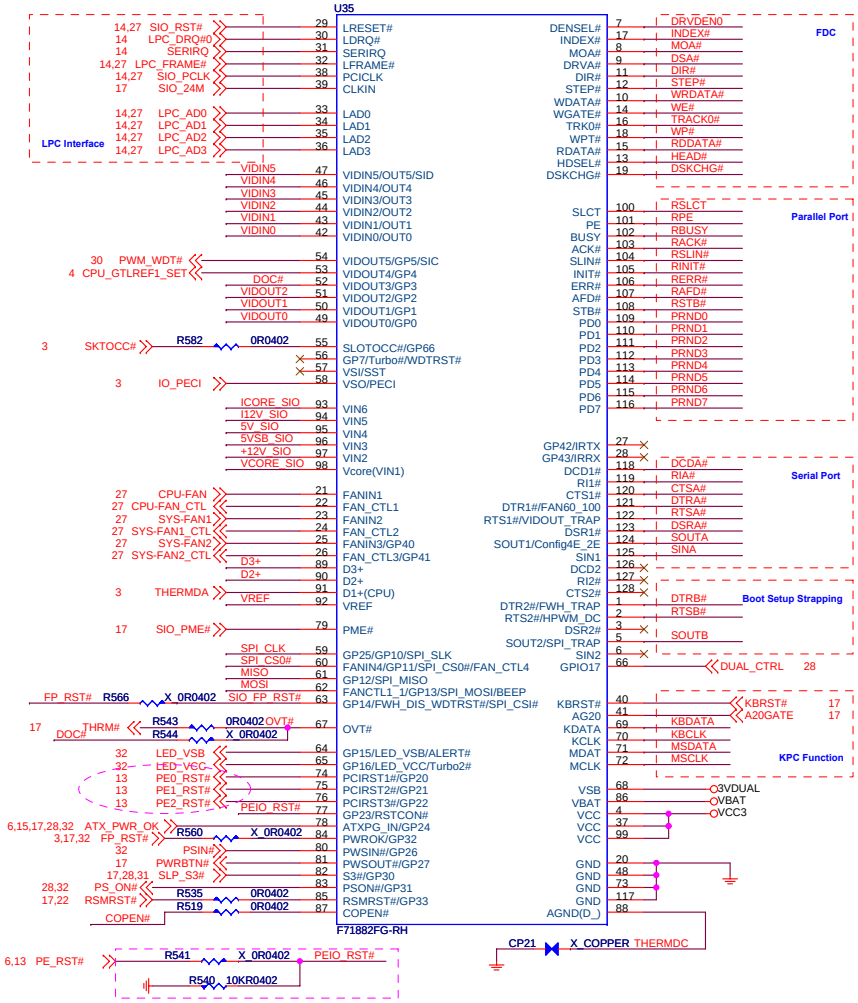
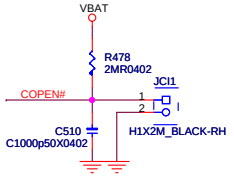
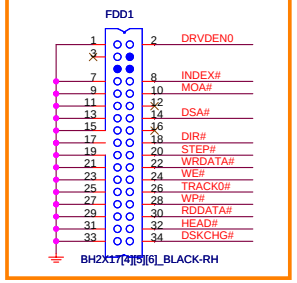
Super I/O FinTek F71882FG



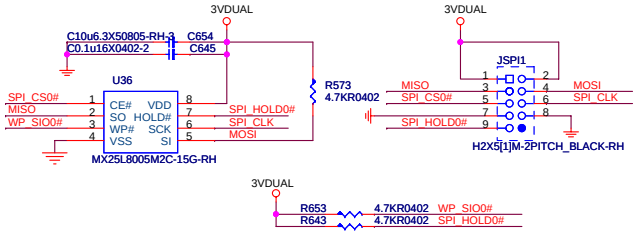
Chasiss Intrusion



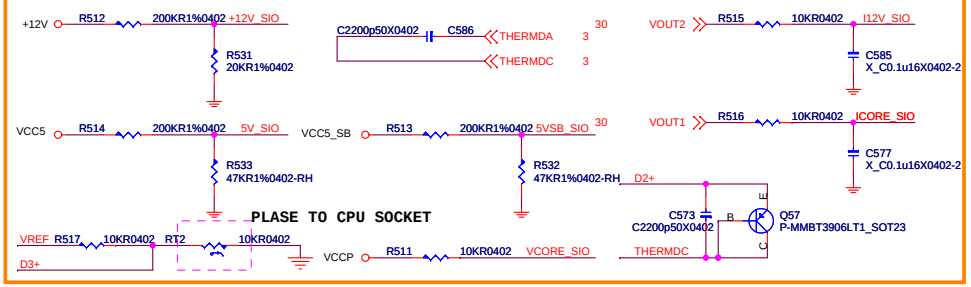
Floppy Connector



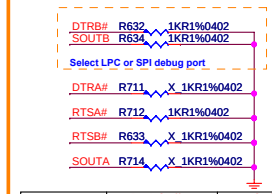
SPI Flash ROM and Debug Port



Voltage and Temperture H/W Monitor Block

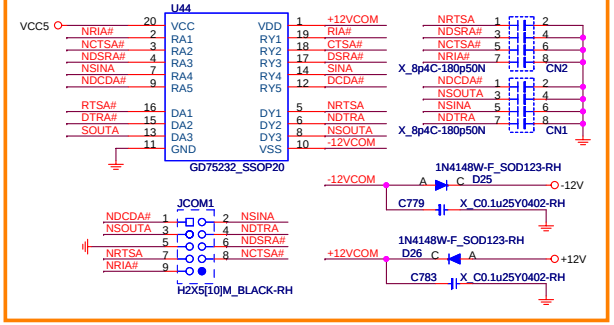


Boot Setup Strapping

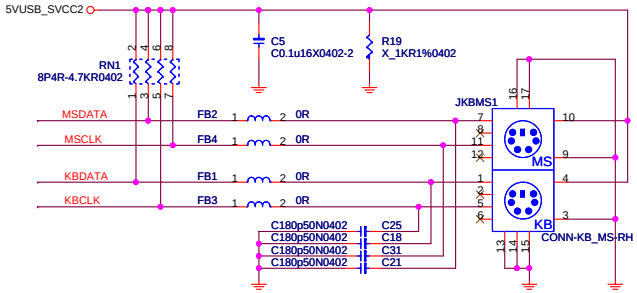


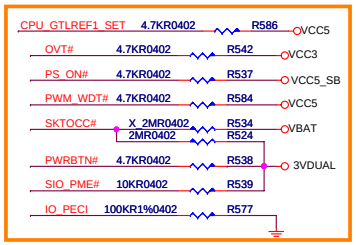
	Don't Stuff	Stuff
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E / 4F	2E / 2F
SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN Start Duty 60%	FAN Start Duty 100%

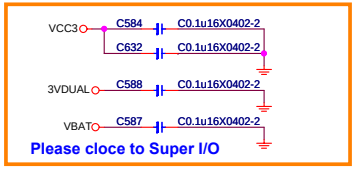
Serial Port (COM1)

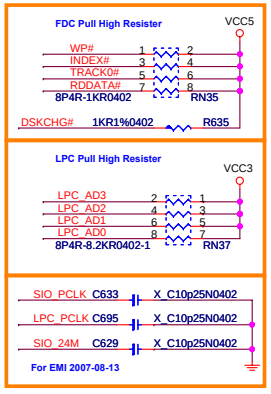


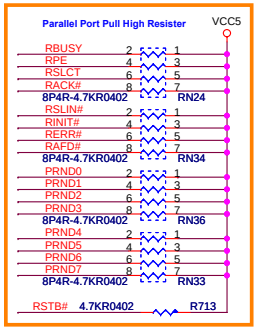
PS2 Keyboard and Mouse Connector

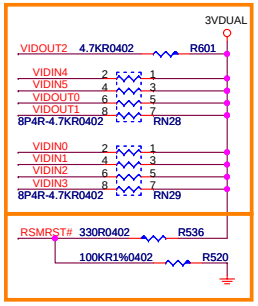






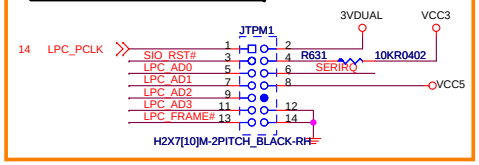






Debug LED Port 1

TPM Module Port



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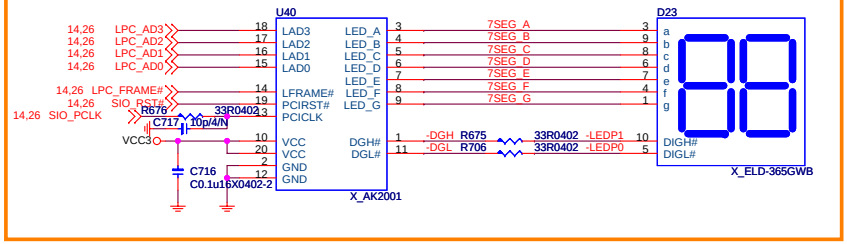
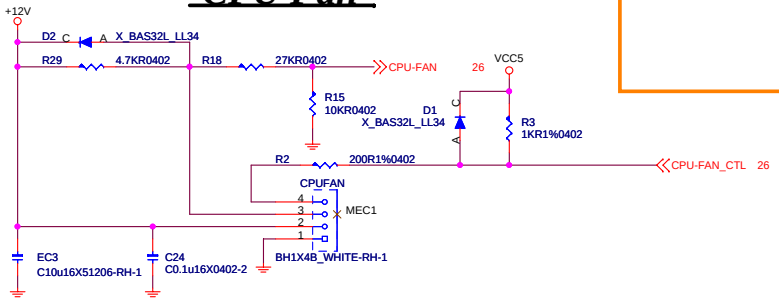
Fan Controller

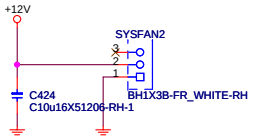
Debug LED Port 2



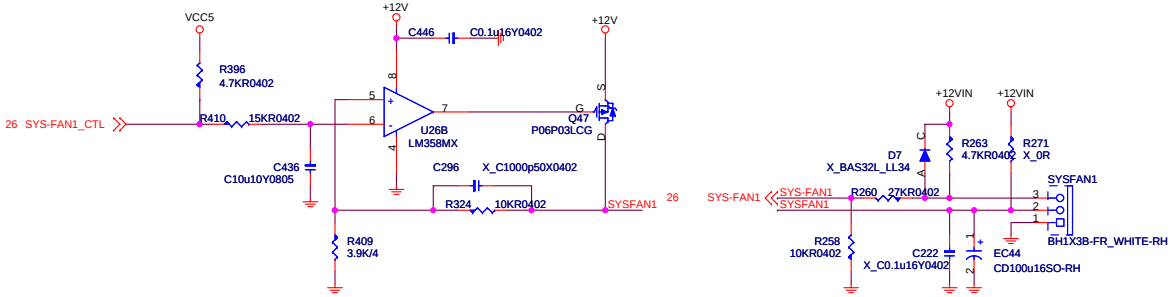
CPU Fan



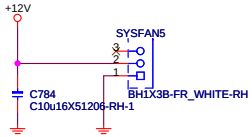
System Fan 3



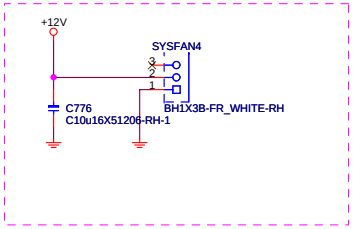
System Fan 1



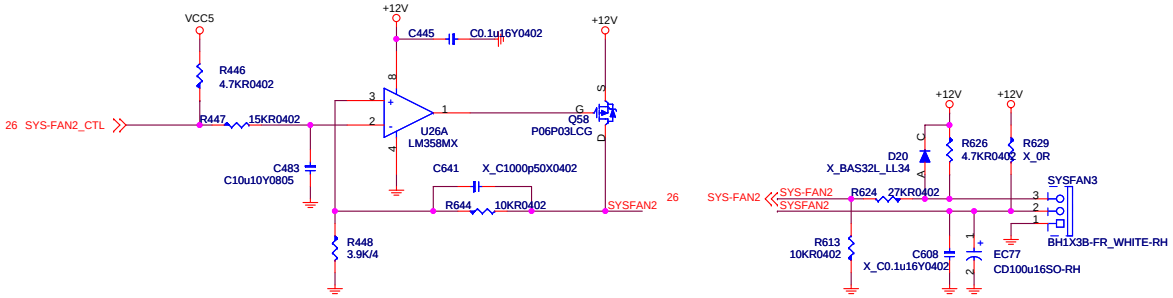
System Fan 4



System Fan 5



System Fan 2



MICRO-START INT'L CO.,LTD.

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Fan Controller		
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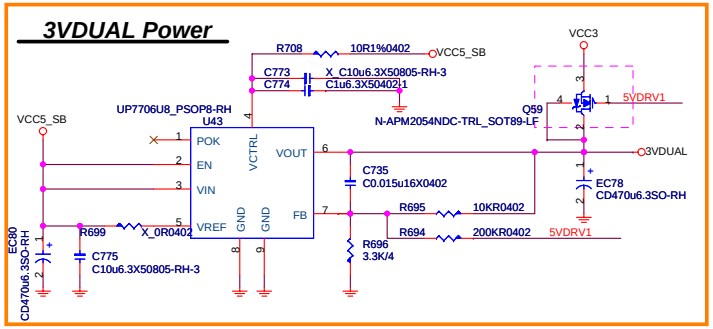
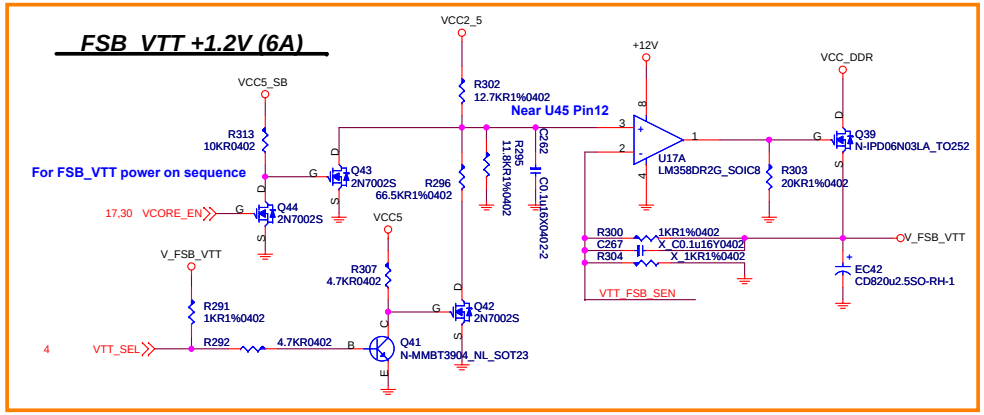
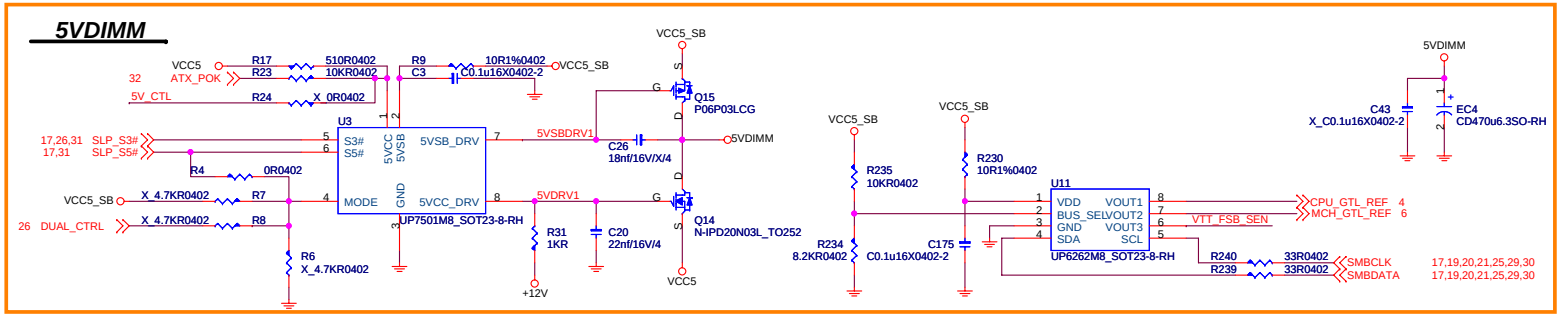
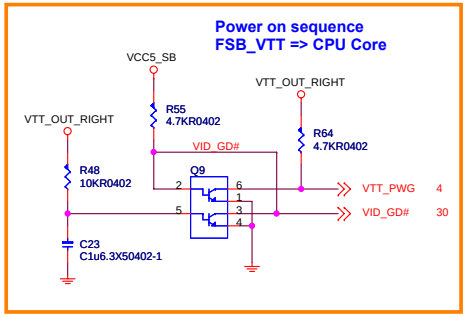
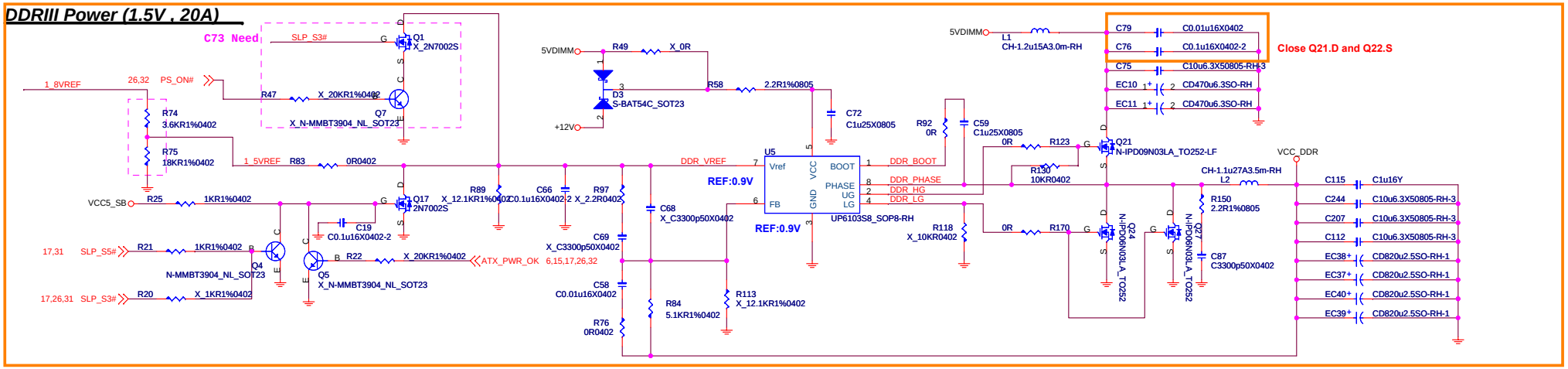
uPI ACPI Solution

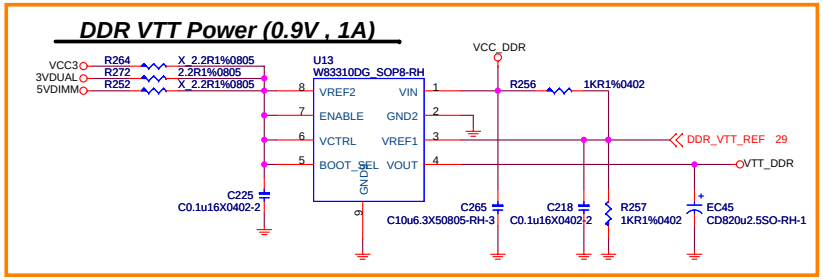


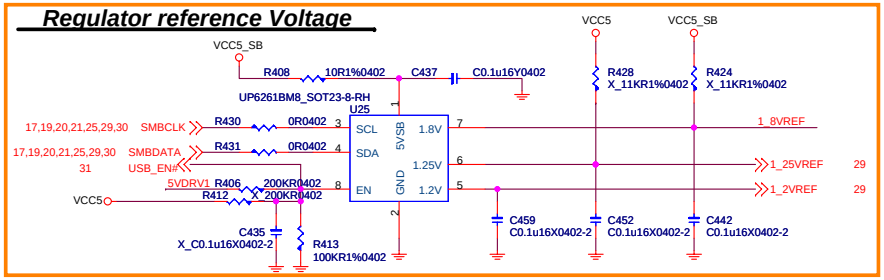


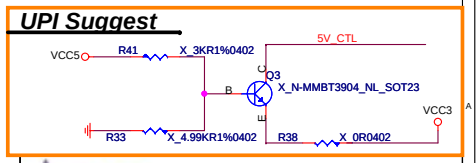












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uPI ACPI Controller		
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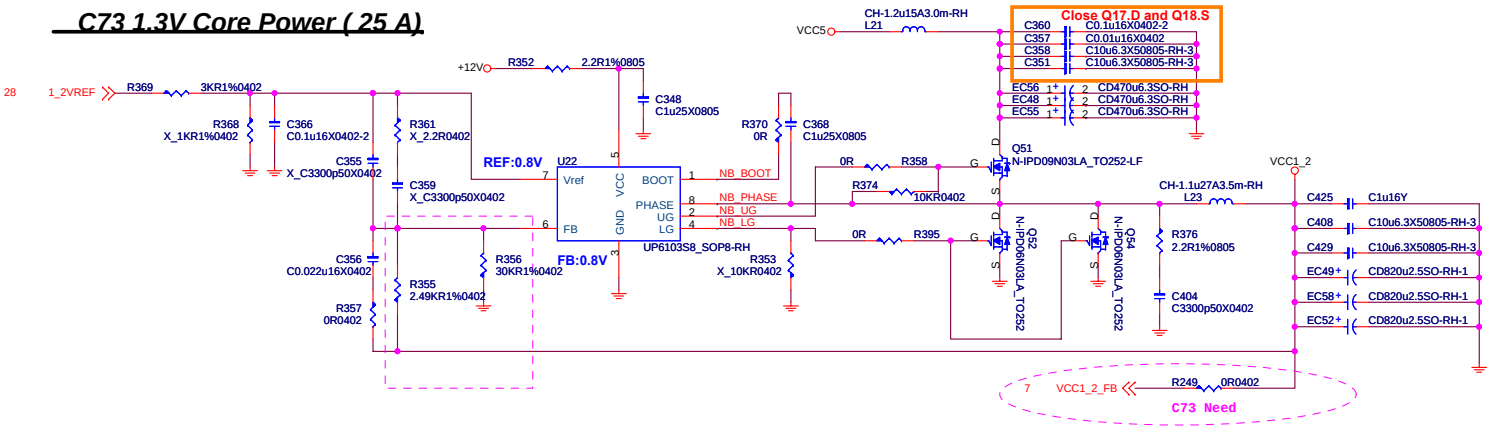
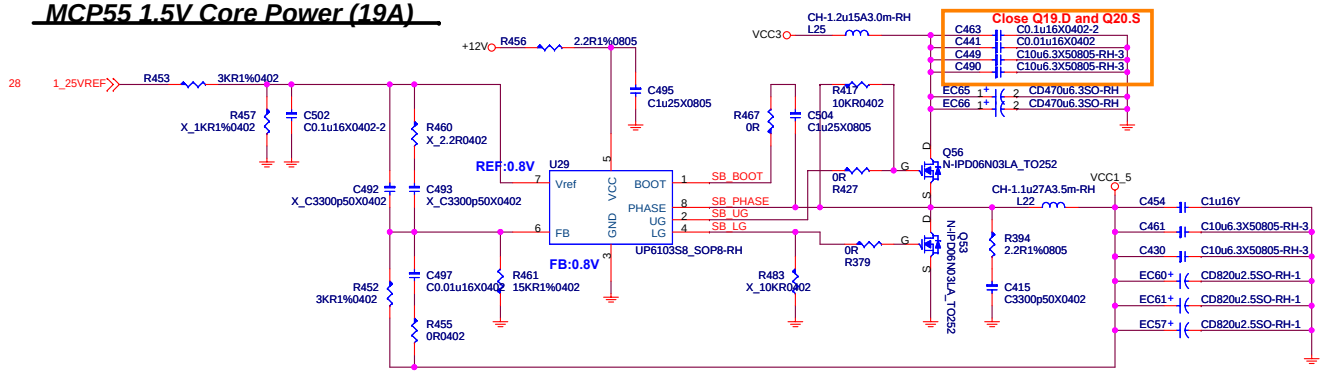
uPI Power Regulator

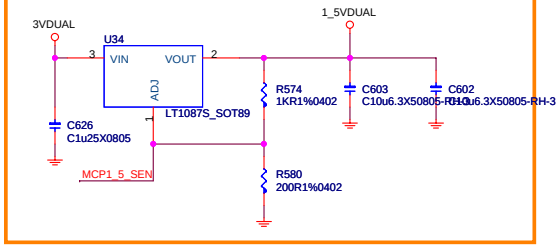
C73 1.3V Core Power (25 A)



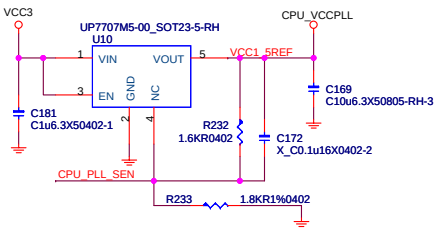
MCP55 1.5V Core Power (19A)



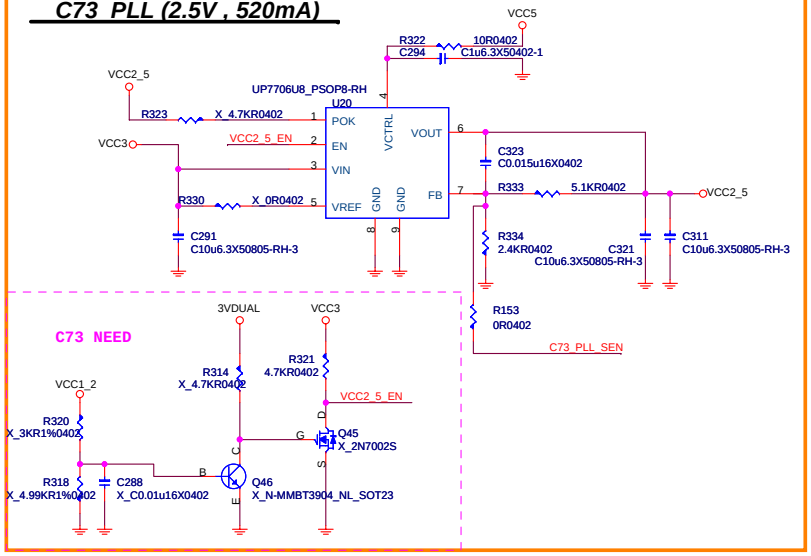
MCP55 1.5V Dual Power (300mA)



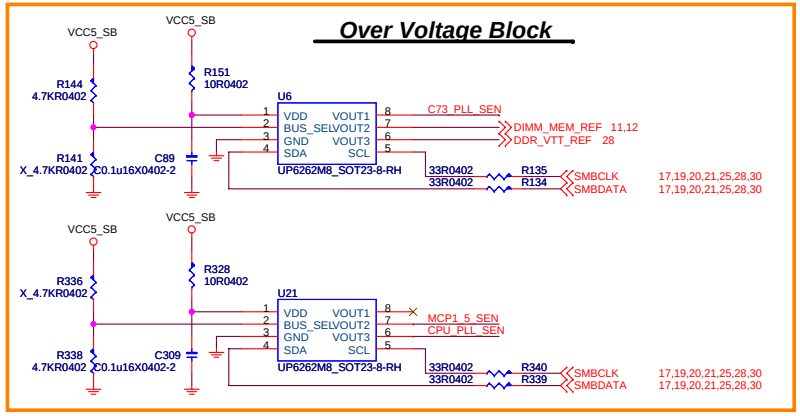
CPU VCCPLL (1.5V 300mA)



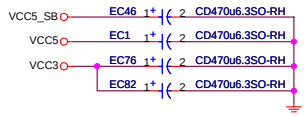
C73 PLL (2.5V , 520mA)



Over Voltage Block



NB +1.2V HT (1.2V 850mA)



MSI Link to the Future MICRO-START INT'L CO.,LTD.

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uPI Power Regulator		
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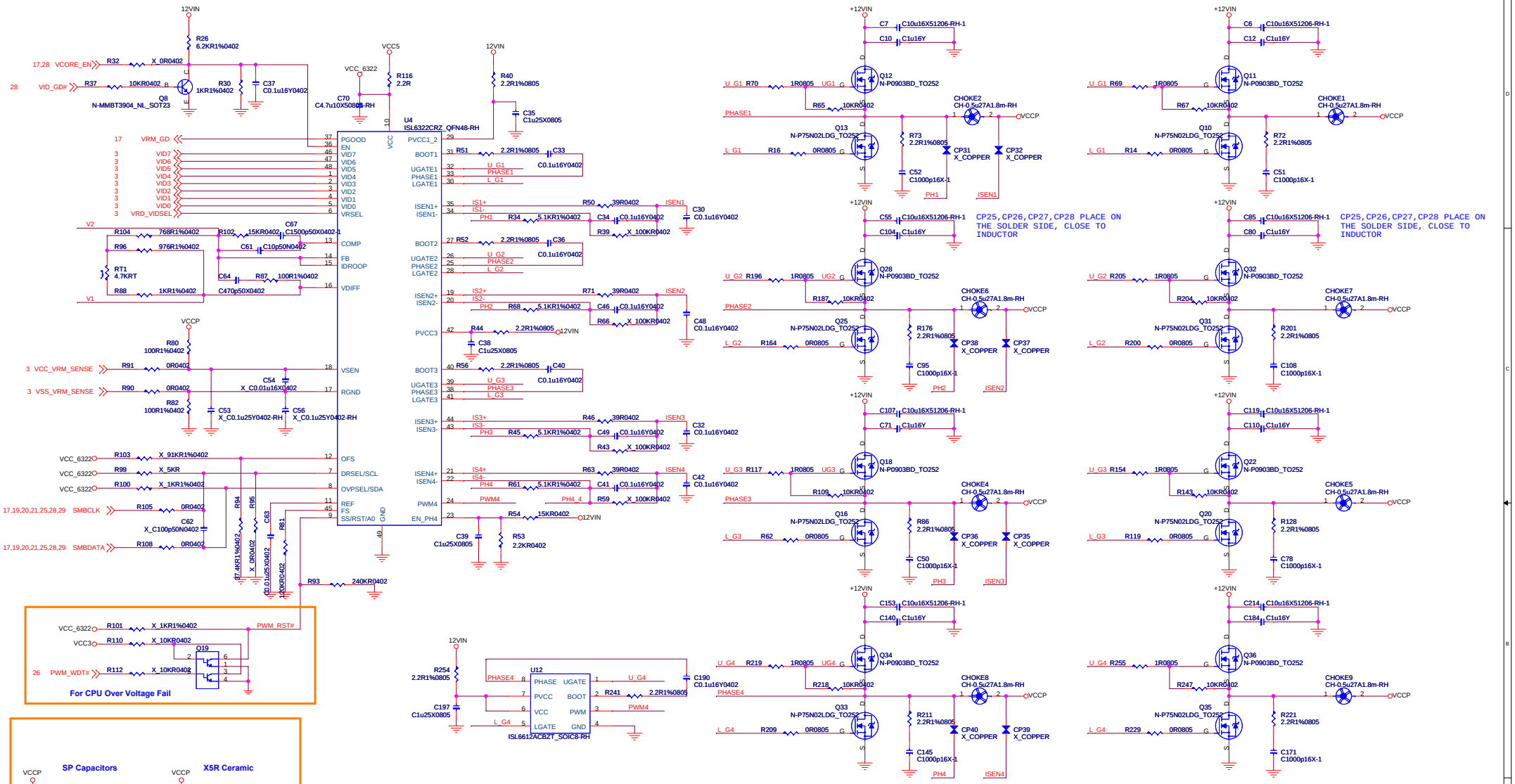
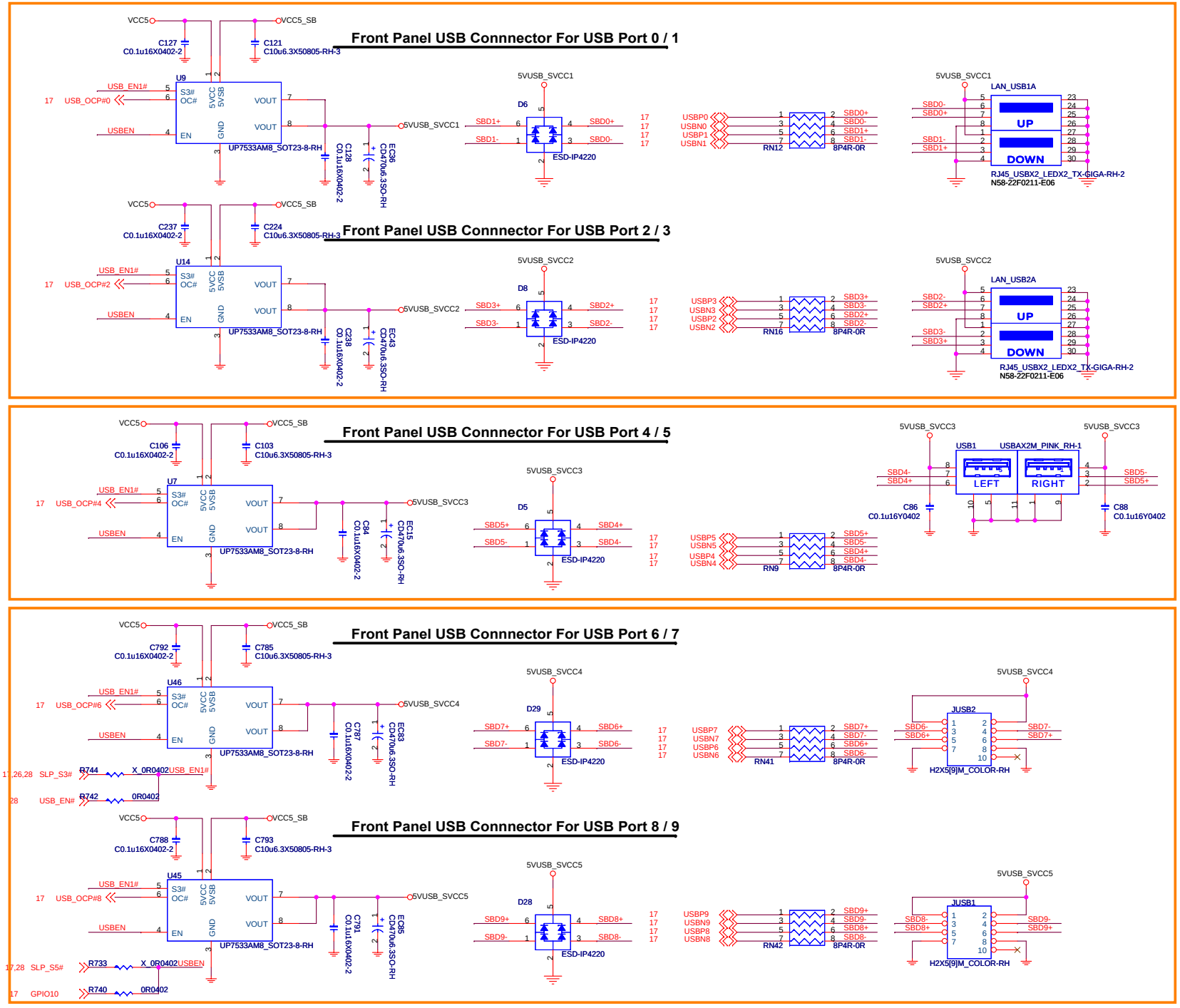
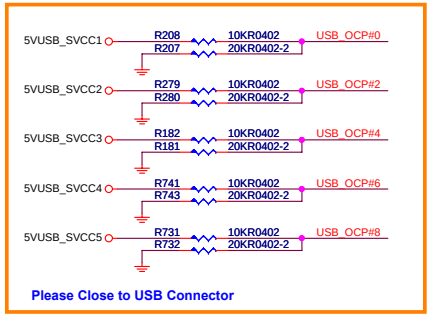
Voltage Regular Module (VRD11)



Front Panel and Real I/O USB Connector





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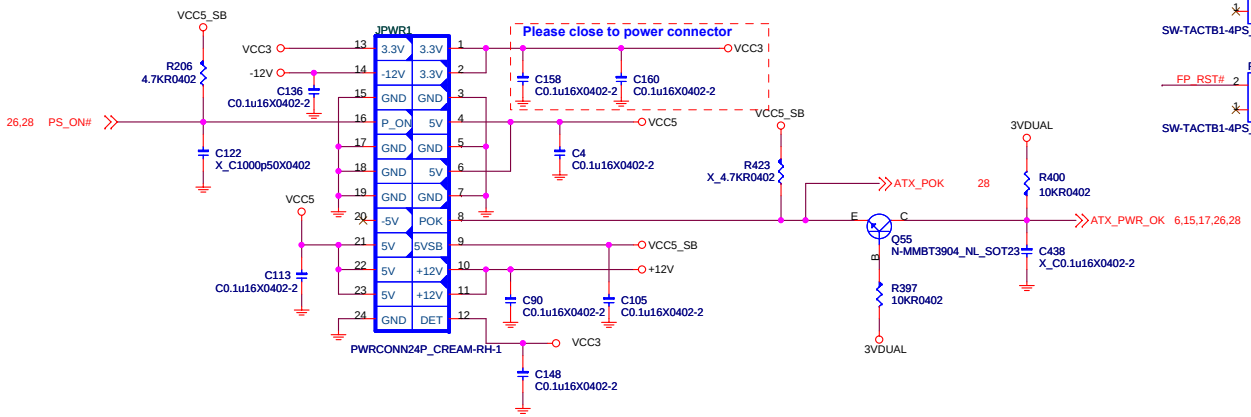
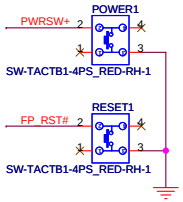
ATX Power Connector / Front Panel / LED

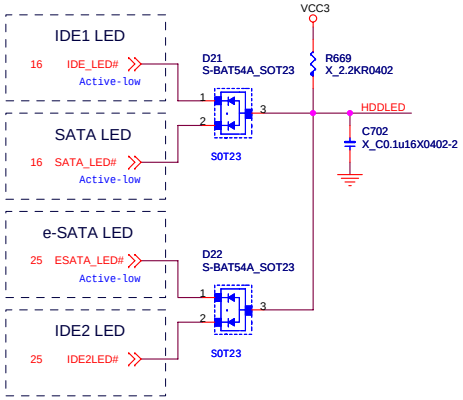
24 Pin ATX Power Connector



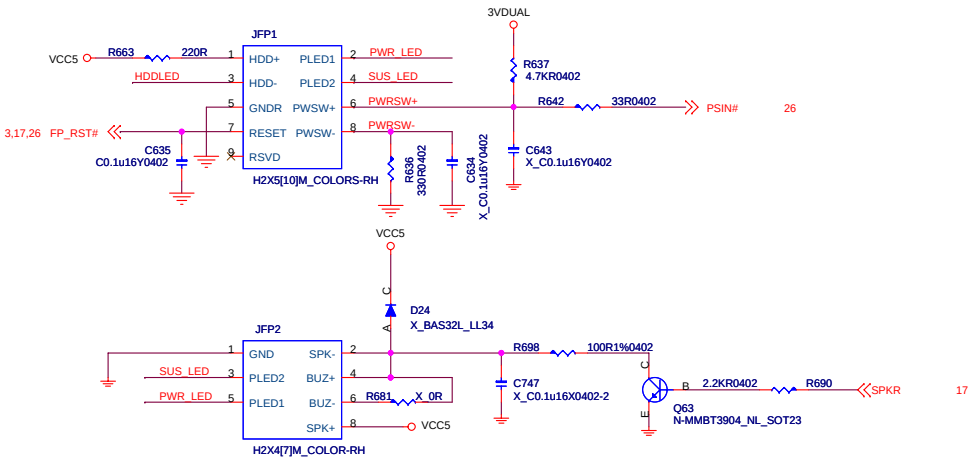
Power and Reset Button

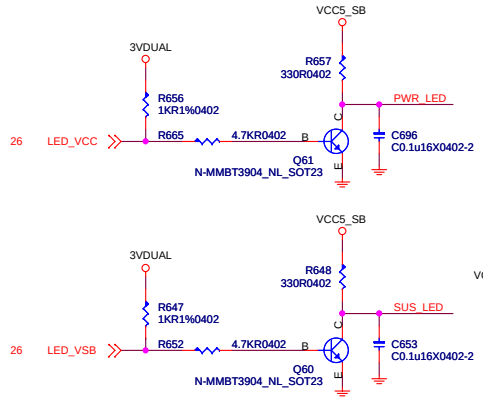


HDD LED



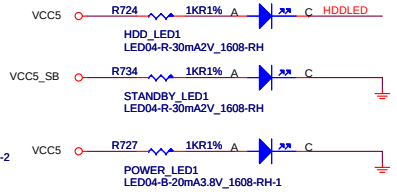
Front Panel





Power State LED

VCC5	BLUE
VCC5_SB	RED
HDD	RED



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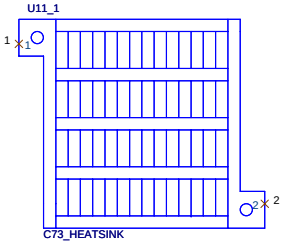

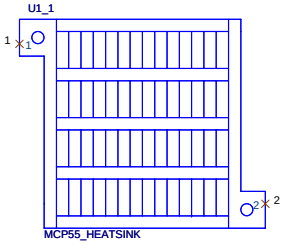

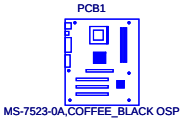

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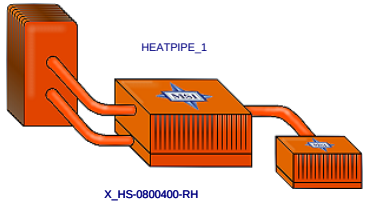
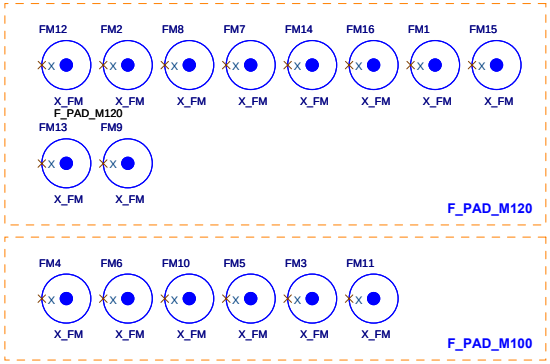
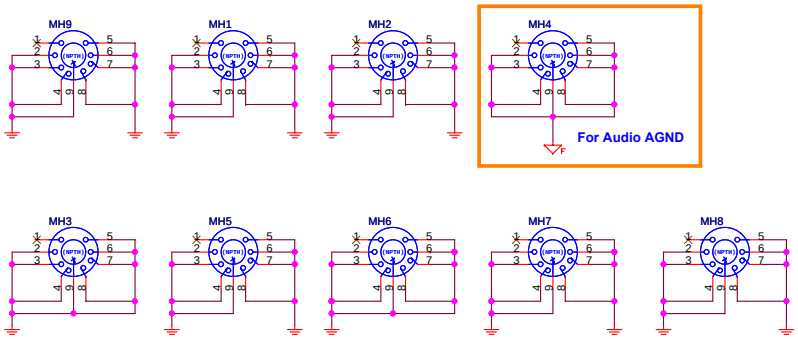


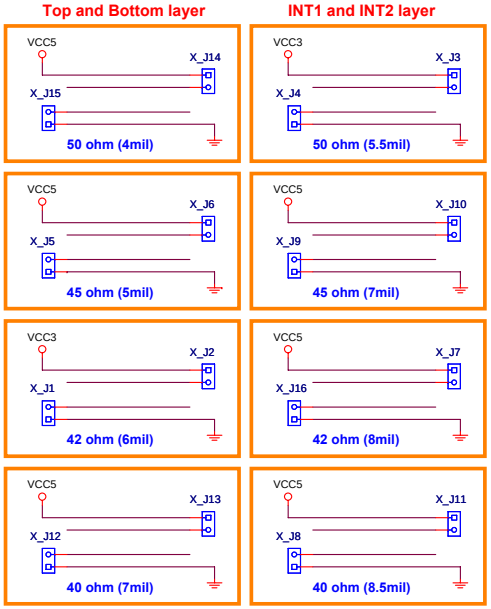
Optics Orientation Holes



PCB Mounting Holes



Simulation



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Manual Parts		
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Power On/Off Sequence

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Title		
	Power On/Off Sequence	
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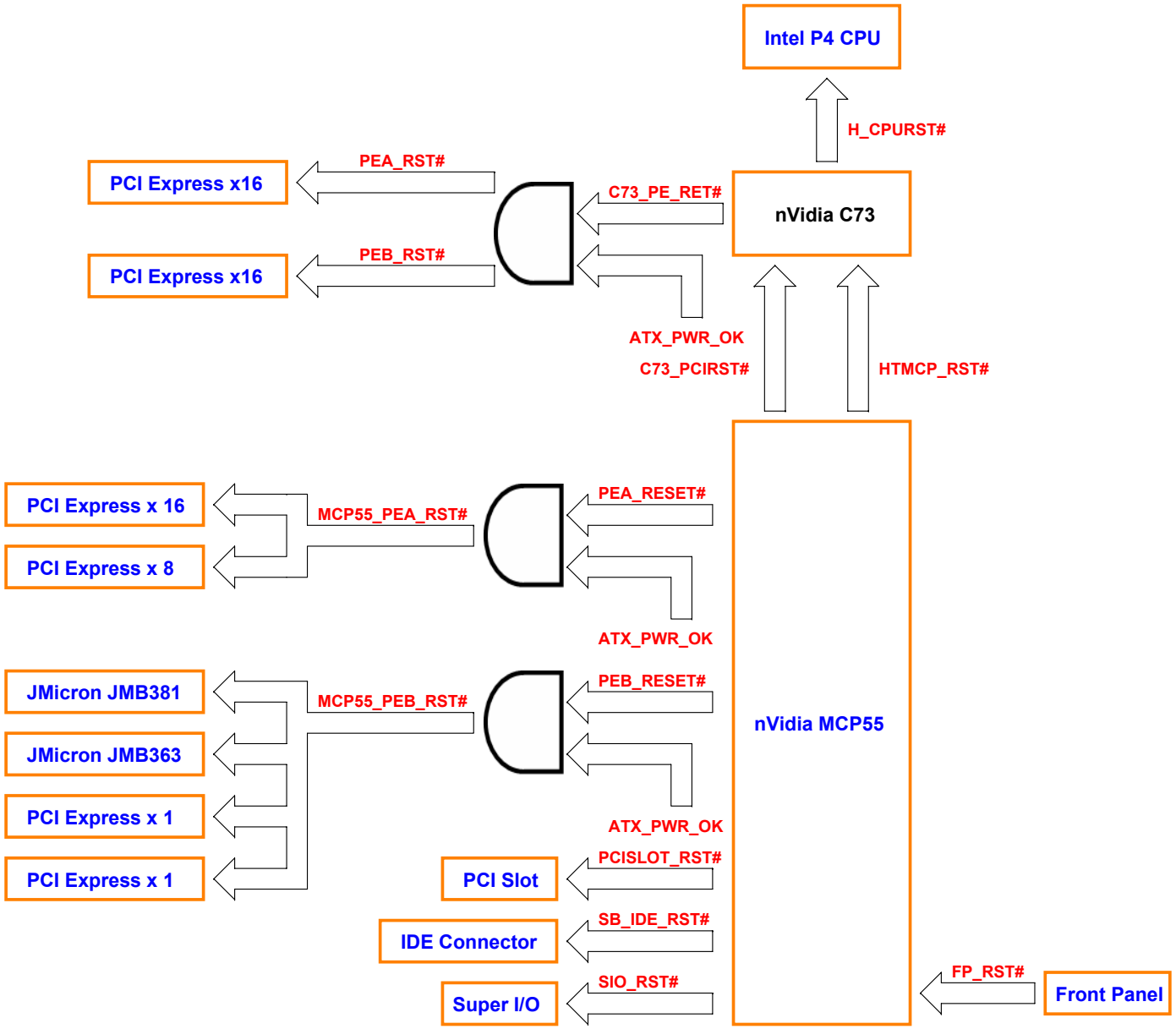
Syatem Reset Map



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title		
Reset Map		
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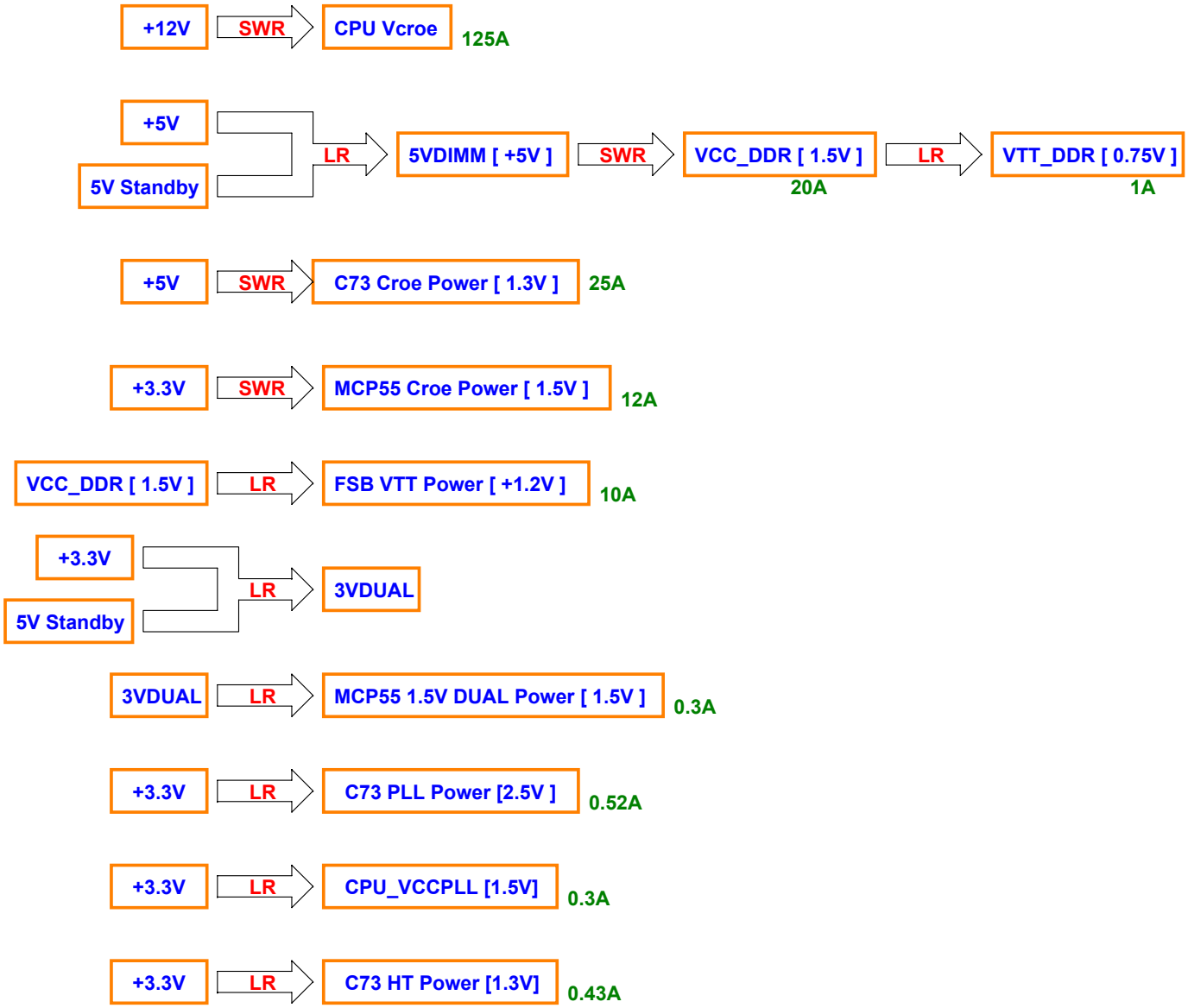
Syatem Power Map



MSI Link to the Future MICRO-START INT'L CO.,LTD.

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Configuration & GPIO

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
PCI slot 1	PIRQ#A	PCI0REQ# PCI0GNT#	AD21	PCI_CLK0	PCISLOT_RST#

DDRII DIMM Configuration

DIMM1	DIMM2	DIMM3	DIMM4
A0 1010000B	A4 1010010B	A2 1010001B	A6 1010011B
0A	0B	1A	1B

SMBus Distribution

SMBus	Power	Load
SMBDATA SMBCLK	VCC3	MCP55 , JM363 , PWM , Super I/O , uPI Power IC PCI Express x16 Slot * 3 , PCI Express x 8 Slot * 1 , PCI Express x 1 Slot * 1 , PCI Slot
SMB_MEM_DATA SMB_MEM_CLK	VCC3_SB	MCP55

System Reset Signal

Signal	Device
PE_RESET#	
H_CPURST#	CPU
HTMCP_RST#	C73
PE_A_RESET#	C73 PCI Express x 16 Primary Slot
PE_B_RESET#	C73 PCI Express x 16 Secondary Slot
PEB_RESET#	JMicron JMB363 eSATA Controller JMicron JMB381 IEEE 1394a Host Controller MCP55 PCI Express x 1 Slot
PEA_RESET#	MCP55 PCI Express x 16 Slot MCP55 PCI Express x 8 Slot
PCISLOT_RST#	MCP55 PCI Slot
C73_PCIRST#	C73
SB_IDE_RST#	Master IDE Connector
SIO_RST#	Super I/O

SuperI/O GPIO Function

Pin Name	Function Description
GP4	CPU_GTL_REF Select
GP5	Reset PWM
SLOTOCC#	Detect CPU remove or not
COPEN#	Detect Case Open or not

MCP55 GPIO Function

Pin Name	Function Description
GP10	USB Connector OC# Detect

Device Clock Signal

Signal	Device
CK_H_CPU# CK_H_CPU	C73 to CPU
HTMCP_DWNCLK0 HTMCP_DWNCLK0#	C73 to MCP55
HTMCP_UPCLK0 HTMCP_UPCLK0#	MCP55 to C73
PE_A_REFCLK PE_A_REFCLK#	C73 to Express x 16 Primary Slo
PE_B_REFCLK PE_B_REFCLK#	C73 to Express x 16 Secondary Slot
MCPOUT_200MHZ MCPOUT_200MHZ#	MCP55 to C73
C73_25MHZ	MCP55 to C73
PE0SB_CLK PE0SB_CLK#	MCP55 to Express x 16 Slot
PE5SB_CLK PE5SB_CLK#	MCP55 to Express x 8 Slot
PE1SB_CLK PE1SB_CLK# PE2SB_CLK PE2SB_CLK#	MCP55 to PCI Express x 1 Slot
PE3SB_CLK PE3SB_CLK#	MCP55 to JMicron JMB363 eSATA Controller
PE4SB_CLK PE4SB_CLK#	MCP55 to JMicron JMB381 IEEE1394a Controller
PCI_CLK0	MCP55 to PCI Slot
SIO_PCLK	MCP55 to FinTek 71883FG Super I/O
LPC_PCLK	MCP55 to JTPM Pin Header

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Title: GPIO & Jumper Setting

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2007-11-05

Crate First Version Schematic

2007-11-10

7523 0A Net-in

2007-11-07

Update project Spec.
From PDC42819 change to JMB363

2007-11-22

Update nVidia PCI Express clock jitter issue solution

2007-11-23

Gerber Out

2007-11-25

Assembly

2007-12-15

HW gat sample board

MICRO-START INT'L CO.,LTD.

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